易 灵 思

T13 Data Sheet

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Introduction

The T13 FPGA features the high-density, low-power Elitestek® Quantum® architecture wrapped with an I/O interface for easy integration. With a high I/O to logic ratio and differential I/O support, T13 FPGAs supports a variety of applications that need wide I/O connectivity. The T13 also includes a MIPI D-PHY with a built-in, royalty-free CSI-2 controller, which is the most popular camera interface used in the mobile industry. The carefully tailored combination of core resources and I/O provides enhanced capability for applications such as embedded vision, voice and gesture recognition, intelligent sensor hubs, power management, and LED drivers.

Features

- High-density, low-power Quantum® architecture
- Built on SMIC 40 nm process
- Core leakage current as low as 6.8 mA(1)
- FPGA interface blocks
  - GPIO
  - PLL
  - LVDS 800 Mbps per lane with up to 13 TX pairs and 13 RX pairs
  - MIPI DPHY with CSI-2 controller hard IP, 1.5 Gbps per lane
- Programmable high-performance I/O
  - Supports 1.8, 2.5, and 3.3 V single-ended I/O standards and interfaces
- Flexible on-chip clocking
  - 16 low-skew global clock signals can be driven from off-chip external clock signals or PLL synthesized clock signals
  - PLL support
- Flexible device configuration
  - Standard SPI interface (active, passive, and daisy chain)
  - JTAG interface
  - Optional Mask Programmable Memory (MPM) capability
- Fully supported by the Efinity® software, an RTL-to-bitstream compiler

Table 1: T13 FPGA Resources

LEs(2)	Global Clock Networks	Global Control Networks	Embedded Memory (kbits)	Embedded Memory Blocks (5 Kbits)	Embedded Multipliers
12,828	Up to 16	Up to 16	727.04	142	24

(1) Typical leakage current for F256 package only.
(2) Logic capacity in equivalent LE counts.

Table 2: T13 Package-Dependent Resources

Resource	Q100F3	F169	F256
Available GPIO[3]	65	73	195
Global clocks from GPIO pins	4	4	16
Global controls from GPIO pins	5	3	16
PLLs	5	5	5
LVDS	4 TX pairs 4 RX pairs	8 TX pairs 12 RX pairs	13 TX pairs 13 RX pairs
MIPI DPHY with CSI-2 controller (4 data lanes, 1 clock lane)	–	2 TX instances 2 RX instances	–

Learn more: Refer to the Trion Packaging User Guide for the package outlines and markings.

Available Package Options

Table 3: Available Packages

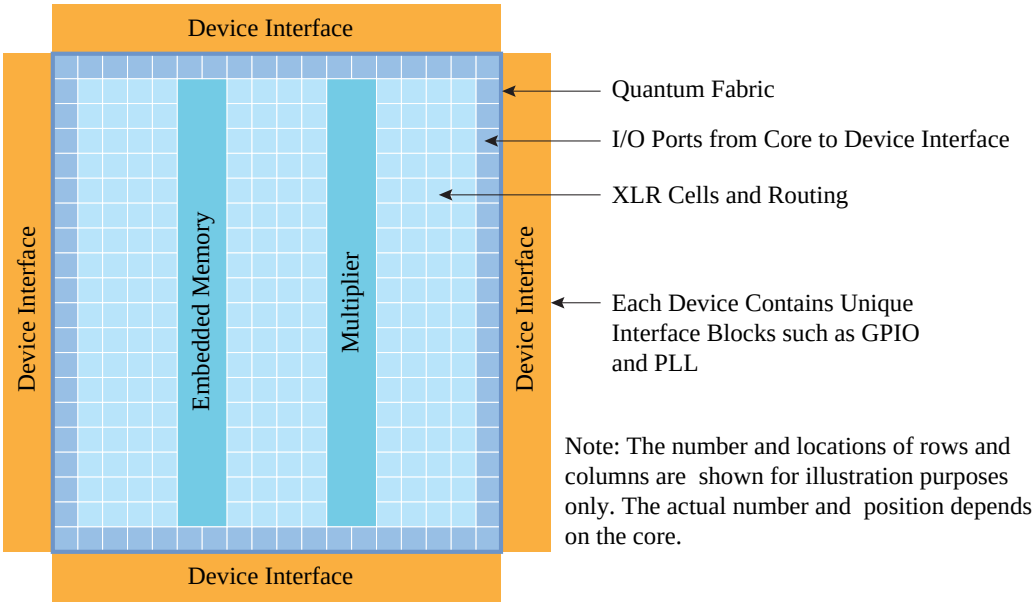
Package	Dimensions (mm x mm)	Pitch (mm)
100-pin LQFP	14 x 14	0.5
169-ball FBGA	9 x 9	0.65
256-ball FBGA	13 x 13	0.8

[3] The LVDS I/O pins are dual-purpose. The full number of GPIO are available when all LVDS I/O pins are in GPIO mode. GPIO and LVDS as GPIO supports different features. See **Table 9: Supported Features for GPIO and LVDS as GPIO** on page 13.

Device Core Functional Description

T13 FPGAs feature an eXchangeable Logic and Routing (XLR) cell that Elitestek has optimized for a variety of applications. Trion® FPGAs contain three building blocks constructed from XLR cells: logic elements, embedded memory blocks, and multipliers. Each FPGA in the Trion® family has a custom number of building blocks to fit specific application needs. As shown in the following figure, the FPGA includes I/O ports on all four sides, as well as columns of XLR cells, memory, and multipliers. A control block within the FPGA handles configuration.

Figure 1: T13 FPGA Block Diagram



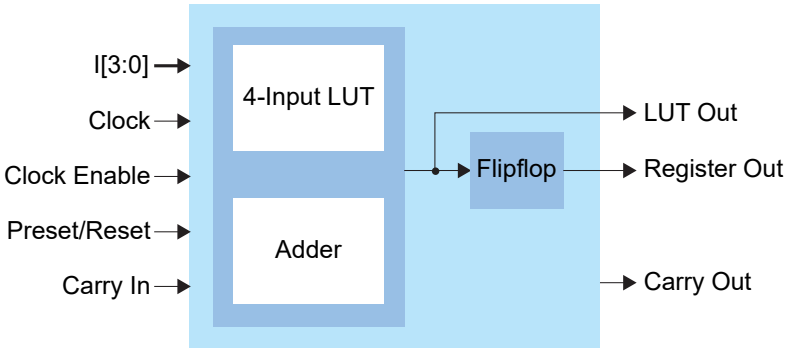
XLR Cell

The eXchangeable Logic and Routing (XLR) cell is the basic building block of the Quantum® architecture. The Elitestek XLR cell combines logic and routing and supports both functions interchangeably. This unique innovation greatly enhances the transistor flexibility and utilization rate, thereby reducing transistor counts and silicon area significantly.

Logic Cell

The logic cell comprises a 4-input LUT or a full adder plus a register (flipflop). You can program each LUT as any combinational logic function with four inputs. You can configure multiple logic cells to implement arithmetic functions such as adders, subtractors, and counters.

Figure 2: Logic Cell Block Diagram



Embedded Memory

The core has 5-kbit high-speed, synchronous, embedded SRAM memory blocks. Memory blocks can operate as single-port RAM, simple dual-port RAM, true dual-port RAM, FIFOs, or ROM. You can initialize the memory content during configuration. The Efinity® software includes a memory cascading feature to connect multiple blocks automatically to form a larger array. This feature enables you to instantiate deeper or wider memory modules.

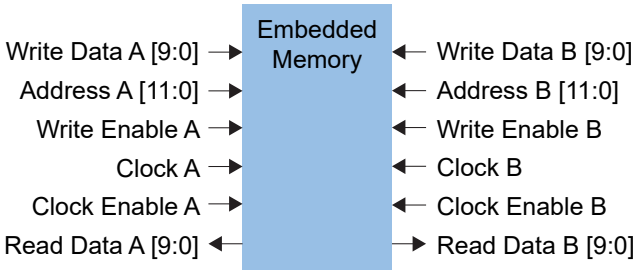
Note: The block RAM content is random and undefined if it is not initialized.

The memory read and write ports have the following modes for addressing the memory (depth x width):

256 x 16	1024 x 4	4096 x 1	512 x 10
512 x 8	2048 x 2	256 x 20	1024 x 5

The read and write ports support independently configured data widths.

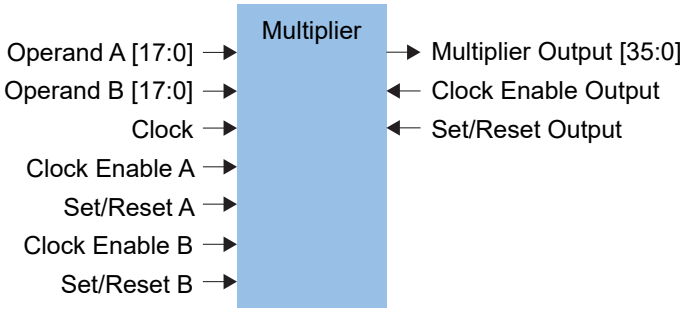
Figure 3: Embedded Memory Block Diagram (True Dual-Port Mode)



Multipliers

The FPGA has high-performance multipliers that support 18 x 18 fixed-point multiplication. Each multiplier takes two signed 18-bit input operands and generates a signed 36-bit output product. The multiplier has optional registers on the input and output ports.

Figure 4: Multiplier Block Diagram

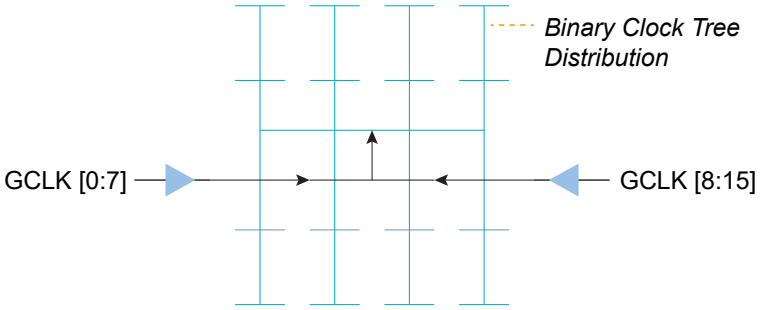


Global Clock Network

The Quantum® core fabric supports up to 16 global clock (GCLK) signals feeding 16 pre-built global clock networks. Global clock pins (GPIO), PLL outputs, and core-generated clocks can drive the global clock network

The global clock networks are balanced clock trees that feed all FPGA modules. Each network has dedicated clock-enable logic to save power by disabling the clock tree at the root. The logic dynamically enables/disables the network and guarantees no glitches at the output.

Figure 5: Global Clock Network



Clock and Control Distribution Network

The global clock network is distributed through the device to provide clocking for the core's LEs, memory, multipliers, and I/O blocks. Designers can access the T13 global clock network using the global clock GPIO pins, PLL outputs, and core-generated clocks. Similarly, the T13 has GPIO pins (the number varies by package) that the designer can configure as control inputs to access the high-fanout network connected to the LE's set, reset, and clock enable signals.

Learn more: Refer to the T13 for information on the location and names of these pins.

Global Clock Location

Table 4: Left Clock Input from GPIO Pins

Function Name	Resource Name	GCLK[0]	GCLK[1]	GCLK[2]	GCLK[3]	GCLK[4]	GCLK[5]	GCLK[6]	GCLK[7]
CLK0	GPIOL_24	✓	–	–	–	✓	–	–	–
CLK1	GPIOL_25	–	✓	–	–	–	✓	–	–
CLK2	GPIOL_26	–	–	✓	–	–	–	✓	–
CLK3	GPIOL_27	–	–	–	✓	–	–	–	✓
CLK4	GPIOL_28	✓	–	–	–	✓	–	–	–
CLK5	GPIOL_29	–	✓	–	–	–	✓	–	–
CLK6	GPIOL_30	–	–	✓	–	–	–	✓	–
CLK7	GPIOL_31	–	–	–	✓	–	–	–	✓

Table 5: Left Clock from PLL OUTCLK Signal

PLL Reference	CLKOUT	GCLK[0]	GCLK[1]	GCLK[2]	GCLK[3]	GCLK[4]	GCLK[5]	GCLK[6]	GCLK[7]
PLL_TL0	CLKOUT0	✓	–	–	–	–	–	✓	–
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–
PLL_TL1	CLKOUT0	–	–	–	✓	–	–	–	✓

PLL Reference	CLKOUT	GCLK[0]	GCLK[1]	GCLK[2]	GCLK[3]	GCLK[4]	GCLK[5]	GCLK[6]	GCLK[7]
	CLKOUT1	–	–	–	–	✓	✓	–	–
	CLKOUT2	–	–	–	–	✓	✓	–	–

Table 6: Right Clock Input from GPIO Pins

Function Name	Resource Name	GCLK[8]	GCLK[9]	GCLK[10]	GCLK[11]	GCLK[12]	GCLK[13]	GCLK[14]	GCLK[15]
CLK0	GPIOR_127	✓	–	–	–	✓	–	–	–
CLK1	GPIOR_126	–	✓	–	–	–	✓	–	–
CLK2	GPIOR_125	–	–	✓	–	–	–	✓	–
CLK3	GPIOR_124	–	–	–	✓	–	–	–	✓
CLK4	GPIOR_123	✓	–	–	–	✓	–	–	–
CLK5	GPIOR_122	–	✓	–	–	–	✓	–	–
CLK6	GPIOR_121	–	–	✓	–	–	–	✓	–
CLK7	GPIOR_120	–	–	–	✓	–	–	–	✓

Table 7: Right Clock from PLL OUTCLK Signal

PLL Reference	CLKOUT	GCLK[8]	GCLK[9]	GCLK[10]	GCLK[11]	GCLK[12]	GCLK[13]	GCLK[14]	GCLK[15]
PLL_TR0	CLKOUT0	✓	–	–	–	–	–	✓	–
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–
PLL_TR1	CLKOUT0	–	–	–	✓	–	–	–	✓
	CLKOUT1	–	–	–	–	✓	✓	–	–
	CLKOUT2	–	–	–	–	✓	✓	–	–
PLL_BR0	CLKOUT0	✓	–	–	–	–	–	–	✓
	CLKOUT1	–	✓	✓	–	–	–	–	–
	CLKOUT2	–	✓	✓	–	–	–	–	–

Device Interface Functional Description

The device interface wraps the core and routes signals between the core and the device I/O pads through a signal interface. Because they use the flexible Quantum® architecture, devices in the Trion® family support a variety of interfaces to meet the needs of different applications.

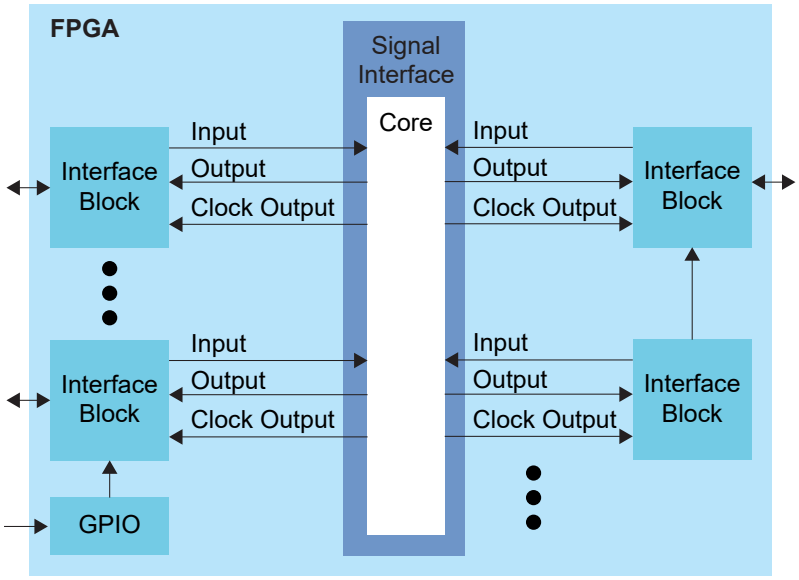
Learn more: The following sections describe the available device interface features in T13 FPGAs. Refer to the Trion® Interfaces User Guide for details on the Efinity® Interface Designer settings.

Interface Block Connectivity

The FPGA core fabric connects to the interface blocks through a signal interface. The interface blocks then connect to the package pins. The core connects to the interface blocks using three types of signals:

- *Input*—Input data or clock to the FPGA core
- *Output*—Output from the FPGA core
- *Clock output*—Clock signal from the core clock tree

Figure 6: Interface Block and Core Connectivity



GPIO blocks are a special case because they can operate in several modes. For example, in alternate mode the GPIO signal can bypass the signal interface and directly feed another interface block. So a GPIO configured as an alternate input can be used as a PLL reference clock without going through the signal interface to the core.

When designing for Trion® FPGAs, you create an RTL design for the core and also configure the interface blocks. From the perspective of the core, outputs from the core are inputs to the interface block and inputs to the core are outputs from the interface block.

The Efinity netlist always shows signals from the perspective of the core, so some signals do not appear in the netlist:

- GPIO used as reference clocks are not present in the RTL design, they are only visible in the interface block configuration of the Efinity® Interface Designer.
- The FPGA clock tree is connected to the interface blocks directly. Therefore, clock outputs from the core to the interface are not present in the RTL design, they are only part of the interface configuration (this includes GPIO configured as output clocks).

The following sections describe the different types of interface blocks. Signals and block diagrams are shown from the perspective of the interface, not the core.

General-Purpose I/O Logic and Buffer

The GPIO support the 3.3 V LVTTL and 1.8 V, 2.5 V, and 3.3 V LVCMOS I/O standards. The GPIOs are grouped into banks. Each bank has its own VCCIO that sets the bank voltage for the I/O standard.

Each GPIO consists of I/O logic and an I/O buffer. I/O logic connects the core logic to the I/O buffers. I/O buffers are located at the periphery of the device.

The I/O logic comprises three register types:

- *Input*—Capture interface signals from the I/O before being transferred to the core logic
- *Output*—Register signals from the core logic before being transferred to the I/O buffers
- *Output enable*—Enable and disable the I/O buffers when I/O used as output

Table 8: GPIO Modes

GPIO Mode	Description
Input	Only the input path is enabled; optionally registered. If registered, the input path uses the input clock to control the registers (positively or negatively triggered). Select the alternate input path to drive the alternate function of the GPIO. The alternate path cannot be registered. In DDIO mode, two registers sample the data on the positive and negative edges of the input clock, creating two data streams.
Output	Only the output path is enabled; optionally registered. If registered, the output path uses the output clock to control the registers (positively or negatively triggered). The output register can be inverted. In DDIO mode, two registers capture the data on the positive and negative edges of the output clock, multiplexing them into one data stream.
Bidirectional	The input, output, and OE paths are enabled; optionally registered. If registered, the input clock controls the input register, the output clock controls the output and OE registers. All registers can be positively or negatively triggered. Additionally, the input and output paths can be registered independently. The output register can be inverted.
Clock output	Clock output path is enabled.

Table 9: Supported Features for GPIO and LVDS as GPIO

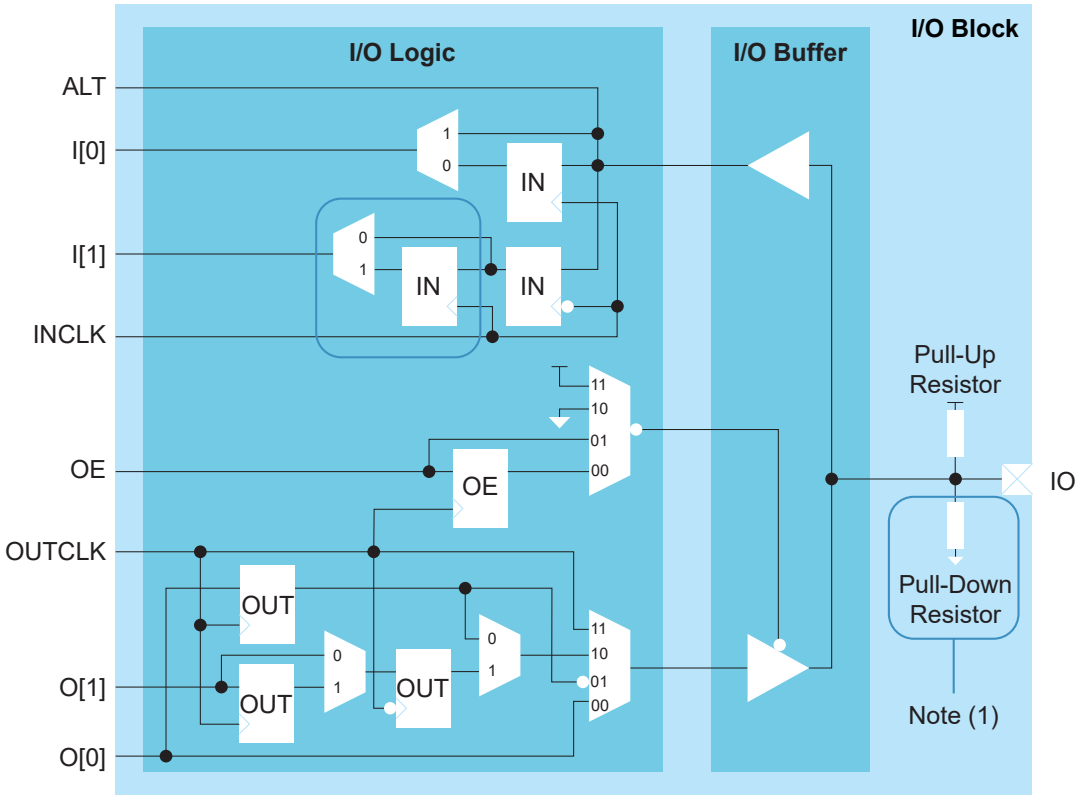
LVDS as GPIO are LVDS pins that act as GPIOs instead of the LVDS function.

Package	GPIO	LVDS as GPIO
Q100F3 F169 F256	DDIO Schmitt Trigger Variable Drive Strength Pull-up Pull-down Slew Rate	Pull-up

Important: Elitestek® recommends that you limit the number of LVDS as GPIO set as output and bidirectional to 16 per bank to avoid switching noise. The Efinity software issues a warning if you exceed the recommended limit.

Complex I/O Buffer

Figure 7: I/O Interface Block



1. GPIO pins using LVDS resources do not have a pull-down resistor.

Note: LVDS as GPIO do not have double data I/O (DDIO).

Table 10: GPIO Signals (Interface to FPGA Fabric)

Signal	Direction	Description
I[1:0]	Output	Input data from the GPIO pad to the core fabric. I[0] is the normal input to the core. In DDIO mode, I[0] is the data captured on the positive clock edge (HI pin name in the Interface Designer) and I[1] is the data captured on the negative clock edge (LO pin name in the Interface Designer).
ALT	Output	Alternative input connection (in the Interface Designer, **Register Option** is **none**). Alternative connections are GCLK, GCTRL, PLL_CLKIN, and MIPI_CLKIN.(4)
O[1:0]	Input	Output data to GPIO pad from the core fabric. O[0] is the normal output from the core. In DDIO mode, O[0] is the data output on the positive clock edge (HI pin name in the Interface Designer) and O[1] is the data output on the negative clock edge (LO pin name in the Interface Designer).
OE	Input	Output enable from core fabric to the I/O block. Can be registered.
OUTCLK	Input	Core clock that controls the output and OE registers. This clock is not visible in the user netlist unless you instantiate an EFX_GPIO_V2 primitive.
INCLK	Input	Core clock that controls the input registers. This clock is not visible in the user netlist unless you instantiate an EFX_GPIO_V2 primitive.

Table 11: GPIO Pads

Signal	Direction	Description
IO	Bidirectional	GPIO pad.

(4) MIPI_CLKIN is only available in packages that support MIPI.

Double-Data I/O

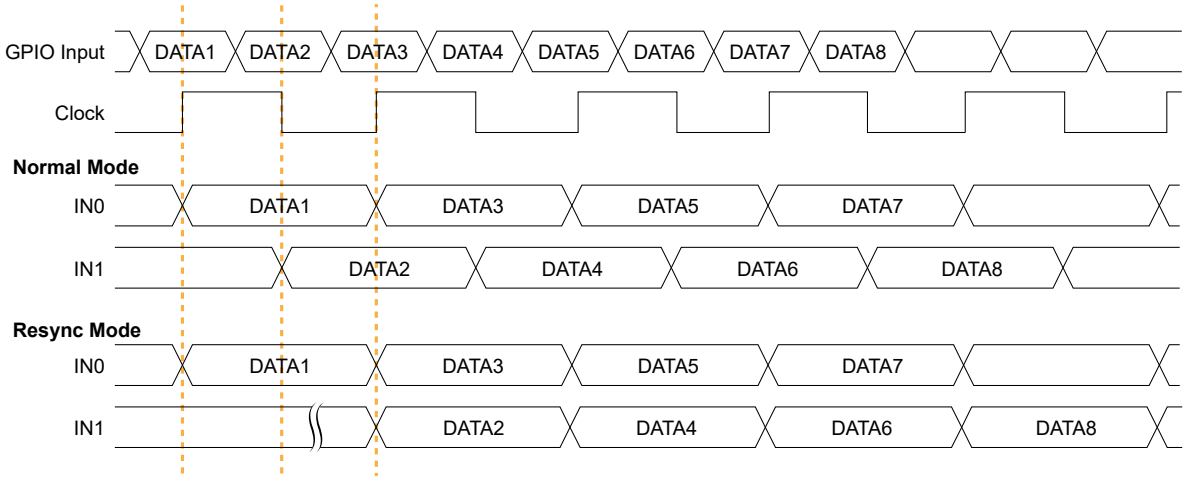
T13 FPGAs support double data I/O (DDIO) on certain input and output registers. In this mode, the DDIO register captures data on both positive and negative clock edges. The core receives 2 bit wide data from the interface.

In normal mode, the interface receives or sends data directly to or from the core on the positive and negative clock edges. In resync mode, the interface resynchronizes the data to pass both signals on the positive clock edge only.

Not all GPIO support DDIO; additionally, LVDS as GPIO (that is, single ended I/O) do not support DDIO functionality.

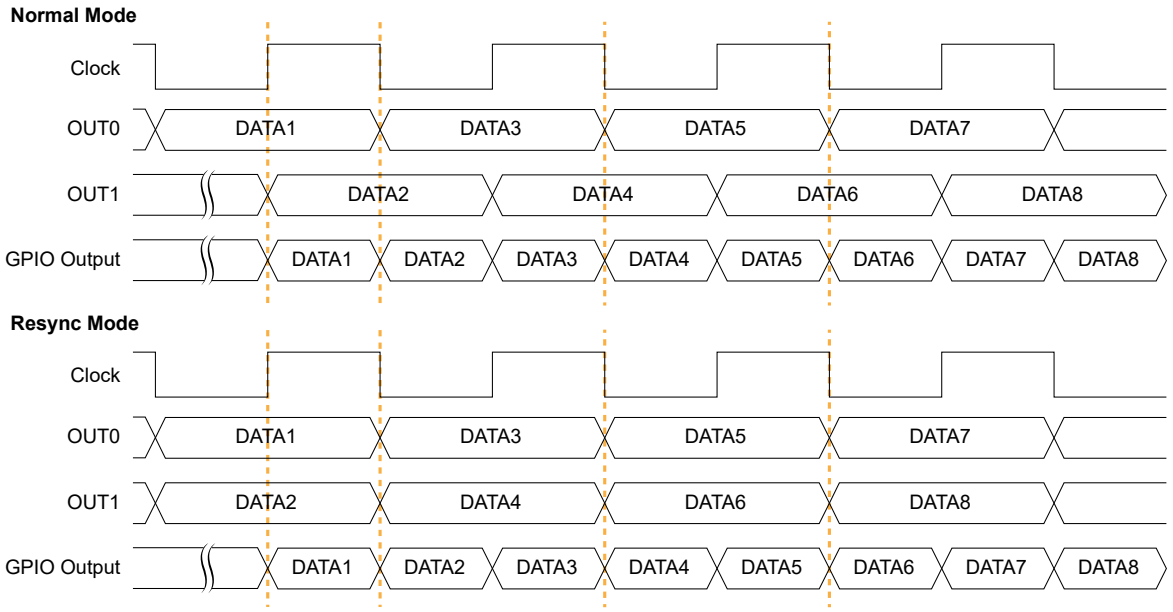
Note: The Resource Assigner in the Efinity® Interface Designer shows which GPIO support DDIO.

Figure 8: DDIO Input Timing Waveform



In resync mode, the IN1 data captured on the falling clock edge is delayed one half clock cycle.
In the Interface Designer, IN0 is the HI pin name and IN1 is the LO pin name.

Figure 9: DDIO Output Timing Waveform



In the Interface Designer, OUT0 is the HI pin name and OUT1 is the LO pin name.

I/O Banks

Elitestek FPGAs have input/output (I/O) banks for general-purpose usage. Each I/O bank has independent power pins. The number and voltages supported vary by FPGA and package.

The number of banks and the voltages they support vary by package.

Some I/O banks are merged at the package level by sharing VCCIO pins. Merged banks have underscores (_) between banks in the name (e.g., 1B_1C means 1B and 1C are connected).

Table 12: I/O Banks by Package

Package	I/O Banks	Voltage (V)	Banks with DDIO Support	Merged Banks
WP80	1A-1E, 3A-3E	1.8, 2.5, 3.3	1B, 1D, 3C, 3D, 3E	1B_1C_1D_1E, 3A_3B_3C, 3D_3E_4A_4B
Q100F3	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1A_1B_1C, 1D_1E, 3B_3C, 3D_3E
	4A, 4B	3.3	–	–
Q144	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1C_1D, 3B_3C
	4A, 4B	3.3	–	–
F169	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1B_1C_1D, 3A_3B, 3C_3D_3E
	4A, 4B	3.3	–	–
F256	1A - 1E, 3A - 3E	1.8, 2.5, 3.3	1B, 1C, 1D, 3B, 3C, 3D, 3E	1B_1C, 1D_1E. 3A_3B_3C, 3D_3E
	4A, 4B	3.3	–	–
F324	1A - 1E, 2A - 2C, 3A - 3C, 4A, 4B, TR, BR	1.8, 2.5, 3.3	1A - 1E, 3C, TR, BR	1B_1C, 1D_1E, 3C_TR_BR
F400	1A - 1E, 2A - 2C, 3C, 4A, 4B, TR, BR	1.8, 2.5, 3.3	1A - 1E, 3C, TR, BR	3C_TR

Learn more: Refer to the T13 for information on the I/O bank assignments.

PLL

The T13 has 5 available PLLs to synthesize clock frequencies.

Note: You can cascade the PLLs in T13 FPGAs. To avoid the PLL losing lock, Elitestek recommends that you do not cascade more than two PLLs.

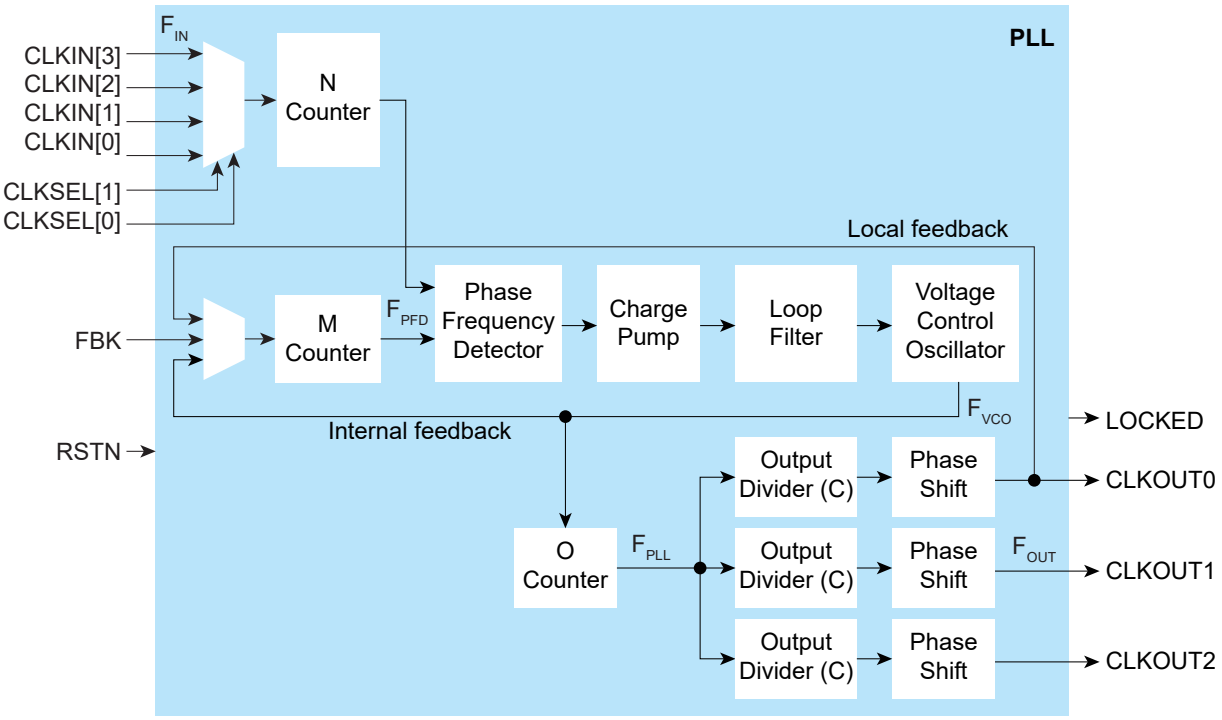
You can use the PLL to compensate for clock skew/delay via external or internal feedback to meet timing requirements in advanced application. The PLL reference clock has up to four sources. You can dynamically select the PLL reference clock with the `CLKSEL` port. (Hold the PLL in reset when dynamically selecting the reference clock source.)

One of the PLLs can use an LVDS RX buffer to input it's reference clock.

The PLL consists of a pre-divider counter (N counter), a feedback multiplier counter (M counter), a post-divider counter (O counter), and output divider.

Note: Refer to T13 Interface Floorplan for the location of the PLLs on the die. Refer to **Table 77: General Pinouts** on page 59 for the PLL reference clock resource assignment.

Figure 10: PLL Block Diagram



The counter settings define the PLL output frequency:

Internal Feedback Mode	Local and Core Feedback Mode	Where:
$F_{PFD} = F_{IN} / N$ $F_{VCO} = F_{PFD} \times M$ $F_{OUT} = (F_{IN} \times M) / (N \times O \times C)$ $F_{PLL} = F_{VCO} / O$	$F_{PFD} = F_{IN} / N$ $F_{VCO} = (F_{PFD} \times M \times O \times C_{FBK})$ [5] $F_{OUT} = (F_{IN} \times M \times C_{FBK}) / (N \times C)$ $F_{PLL} = F_{VCO} / O$	F_{VCO} is the voltage control oscillator frequency F_{OUT} is the output clock frequency F_{IN} is the reference clock frequency F_{PFD} is the phase frequency detector input frequency F_{PLL} is the post-divider PLL frequency C is the output divider O is the post-divider M is the multiplier N is the pre-divider C_{FBK} is the output divider for CLKOUT0

[5] $(M \times O \times C_{FBK})$ must be ≤ 255.

Note: F_{IN} must be within the values stated in **PLL Timing and AC Characteristics** on page 52.

Figure 11: PLL Interface Block Diagram

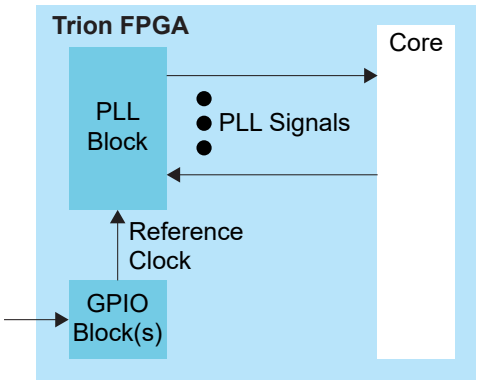


Table 13: PLL Signals (Interface to FPGA Fabric)

Signal	Direction	Description
CLKIN[3:0]	Input	Reference clocks driven by I/O pads or core clock tree.
CLKSEL[1:0]	Input	You can dynamically select the reference clock from one of the clock in pins.
RSTN	Input	Active-low PLL reset signal. When asserted, this signal resets the PLL; when de-asserted, it enables the PLL. De-assert only when the CLKIN signal is stable. Connect this signal in your design to power up or reset the PLL. Assert the RSTN pin for a minimum pulse of 10 ns to reset the PLL. Assert RSTN when dynamically changing the selected PLL reference clock.
FBK	Input	Connect to a clock out interface pin when the PLL feedback mode is not **internal**.
CLKOUT0 CLKOUT1 CLKOUT2	Output	PLL output. The designer can route these signals as input clocks to the core's GCLK network.
LOCKED[6]	Output	Goes high when PLL achieves lock; goes low when a loss of lock is detected; remains at previous state if the CLKIN goes discontinuous. Connect this signal in your design to monitor the lock status. This signal is not synchronized to any clock and the minimum high or low pulse width of the lock signal may be smaller than the CLKOUT's period.

Table 14: PLL Interface Designer Settings - Properties Tab

Parameter	Choices	Notes
Instance Name	User defined	
PLL Resource		The resource listing depends on the FPGA you choose.
Clock Source	External	PLL reference clock comes from external source through the REFCLK pin. Select the available external clock.
	Dynamic	PLL reference clock comes from up to four possible sources (external and core), and are controlled by the clock select bus. Specify the clock selector and core clock names.
	Core	PLL reference clock comes from the core. Specify the core clock pin name.
Automated Clock Calculation		Pressing this button launches the PLL Clock Caclulation window. The calculator helps you define PLL settings in an easy-to-use graphical interface.

[6] The circuitry that generates the lock signal relies on a reference clock edge to transition the lock signal. A sudden removal of the reference clock will result in there being no positive clock edge with which to change the lock state from 1 back to 0. Therefore, the lock signal will remain on 1.

Table 15: PLL Interface Designer Settings - Manual Configuration Tab

Parameter	Choices	Notes
Reset Pin Name	User defined	
Locked Pin Name	User defined	
Feedback Mode	Internal	PLL feedback is internal to the PLL resulting in no known phase relationship between clock in and clock out.
	Local	PLL feedback is local to the PLL. Aligns the clock out phase with clock in.
	Core	PLL feedback is from the core. The feedback clock is defined by the COREFBK connection, and must be one of the three PLL output clocks. Aligns the clock out phase with clock in and removes the core clock delay.
Reference clock Frequency (MHz)	User defined	
Multiplier (M)	1 - 255 (integer)	M counter.
Pre Divider (N)	1 - 15 (integer)	N counter.
Post Divider (O)	1, 2, 4, 8	O counter. The value must be 2 or higher if you enable more than 1 PLL output.
Clock 0, Clock 1, Clock 2	On, off	Use these checkboxes to enable or disable clock 0, 1, and 2.
Pin Name	User defined	Specify the pin name for clock 0, 1, or 2.
Divider (C)	1 to 256	Output divider.
Phase Shift (Degree)	0, 45, 90, 135, 180, or 270	Phase shift CLKOUT by 45°, 90°, 135°, 180°, or 270°. The phase shifts are supported with the following C divider settings: C divider = 2 : 90°, 180°, and 270° C divider = 4 : 45°, 90°, and 135° C divider = 6 : 90° To phase shift 225°, select 45° and invert the clock at the destination. To phase shift 315°, select 135° and invert the clock at the destination.
Use as Feedback	On, off	

Table 16: PLL Reference Clock Resource Assignments

PLL	REFCLK1	REFCLK2
PLL_BR0	Differential: GPIOB_CLKP0, GPIOB_CLKN0 Single Ended: GPIOB_CLKP0	GPIOR_157_PLLIN
PLL_TR0	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TR1	GPIOR_76_PLLIN0	GPIOR_77_PLLIN1
PLL_TL0	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1
PLL_TL1	GPIOL_74_PLLIN0	GPIOL_75_PLLIN1

LVDS

The LVDS hard IP transmitters and receivers operate independently.

- LVDS TX consists of LVDS transmitter and serializer logic.
- LVDS RX consists of LVDS receiver, on-die termination, and de-serializer logic.

The T13 has one PLL for use with the LVDS receiver.

Note: You can use the LVDS TX and LVDS RX channels as 3.3 V single-ended GPIO pins, which support a weak pull-up but do not support a Schmitt trigger or variable drive strength. When using LVDS as GPIO, make sure to leave at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS pins. This rule applies for pins on each side of the device (top, bottom, left, right). This separation reduces noise. The Efinity software issues an error if you do not leave this separation.

The LVDS hard IP has these features:

- Up to 800 Mbps for LVDS data transmit or receive

- Supports serialization and deserialization factors: 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1
- Ability to disable serialization and deserialization
- Source synchronous clock output edge-aligned with data for LVDS transmitter and receiver
- 100 Ω on-die termination resistor for the LVDS receiver

Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

LVDS TX

Figure 12: LVDS TX Interface Block Diagram

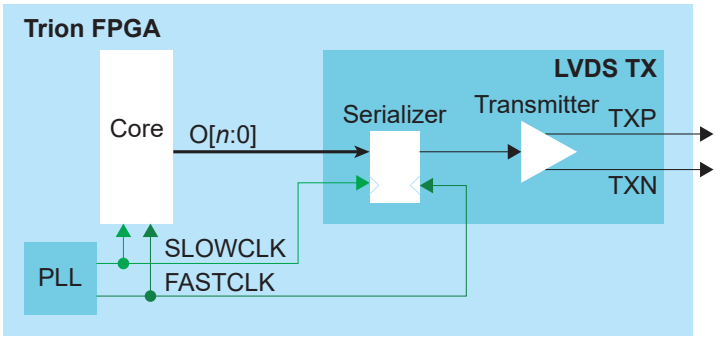


Table 17: LVDS TX Signals (Interface to FPGA Fabric)

Signal	Direction	Notes
O[*n*-1:0]	Input	Parallel output data where *n* is the serialization factor. A width of 1 bypasses the serializer.
FASTCLK	Input	Fast clock to serialize the data to the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data from the core.

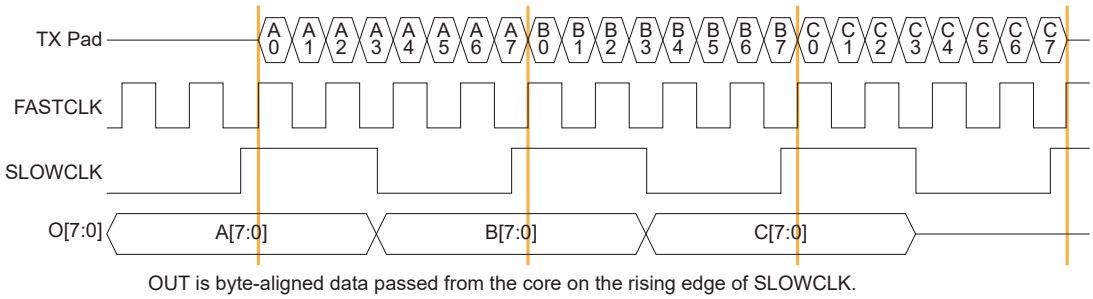
Table 18: LVDS TX Pads

Pad	Direction	Description
TXP	Output	Differential P pad.
TXN	Output	Differential N pad.

Important: For QFP100F3 packages, do not toggle the CCK pin when any LVDS TX is used.

The following waveform shows the relationship between the fast clock, slow clock, TX data going to the pad, and byte-aligned data from the core.

Figure 13: LVDS Timing Example Serialization Width of 8



OUT is byte-aligned data passed from the core on the rising edge of SLOWCLK.

Figure 14: LVDS Timing Data and Clock Relationship Width of 8 (Parallel Clock Division=1)

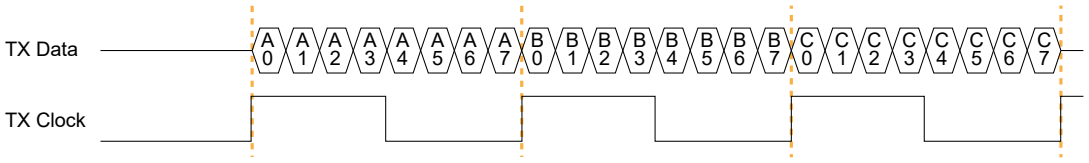
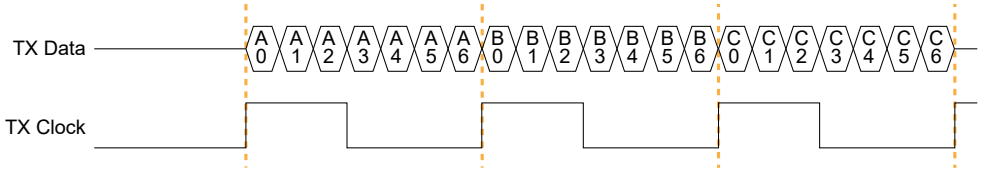


Figure 15: LVDS Timing Data and Clock Relationship Width of 7 (Parallel Clock Division=1)



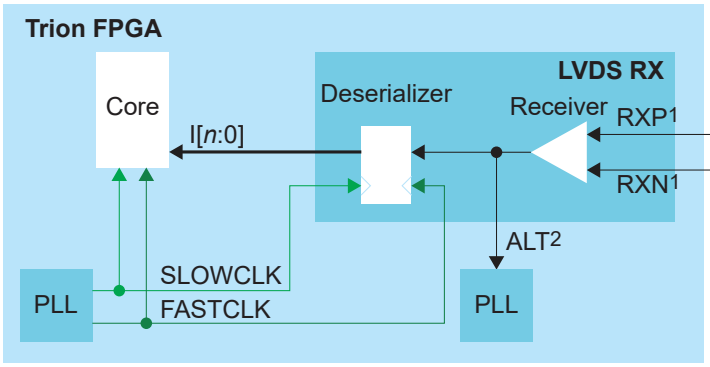
Note: For LVDS TX interfaces with multiple LVDS TX lanes and an LVDS TX reference clock output, use the LVDS TX blocks from the same side of the FPGA to minimize skew between data lanes and TX reference clock output.

Table 19: LVDS TX Settings in Efinity® Interface Designer

Parameters	Choices	Notes
Instance Name	User defined	
LVDS Resource	Resource list	Choose a resource.
Mode	serial data output or reference clock output	**serial data output**—Simple output buffer or serialized output. **reference clock output**—Use the transmitter as a clock output. When choosing this mode, the **Serialization Width** you choose should match the serialization for the rest of the LVDS bus.
Parallel Clock Division	1, 2	**1**—The output clock from the LVDS TX lane is parallel clock frequency. **2**—The output clock from the TX lane is half of the parallel clock frequency.
Enable Serialization	On or off	When off, the serializer is bypassed and the LVDS buffer is used as a normal output.
Serialization Width	2, 3, 4, 5, 6, 7, or 8	Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1. Specify the serial clock and parallel clock.
Output Pin/Bus Name	User defined	Output pin or bus that feeds the LVDS transmitter parallel data. The width should match the serialization factor.
Output Enable Pin Name	User defined	Use with serial data output mode. Only available when serialization is disabled.
Reduce VOD Swing	On or off	When true, enables reduced output swing (similar to slow slew rate).
Output Load	3, 5, 7, or 10	Output load in pF. Use an output load of 7 pF or higher to achieve the maximum supported toggle rate. See **Table 53: Maximum Toggle Rate** on page 45.

LVDS RX

Figure 16: LVDS RX Interface Block Diagram



1. There is a ~30k Ω internal weak pull-up to VCCIO (3.3V).
2. Only available for an LVDS RX resource in bypass mode (deserialization width is 1).

Table 20: LVDS RX Signals (Interface to FPGA Fabric)

Signal	Direction	Notes
I[*n*-1:0]	Output	Parallel input data where *n* is the de-serialization factor. A width of 1 bypasses the deserializer.
ALT	Output	Alternative input, only available for an LVDS RX resource in bypass mode (deserialization width is 1; alternate connection type). Alternative connections are PLL_CLKIN.
FASTCLK	Input	Fast clock to de-serialize the data from the LVDS pads.
SLOWCLK	Input	Slow clock to latch the incoming data to the core.

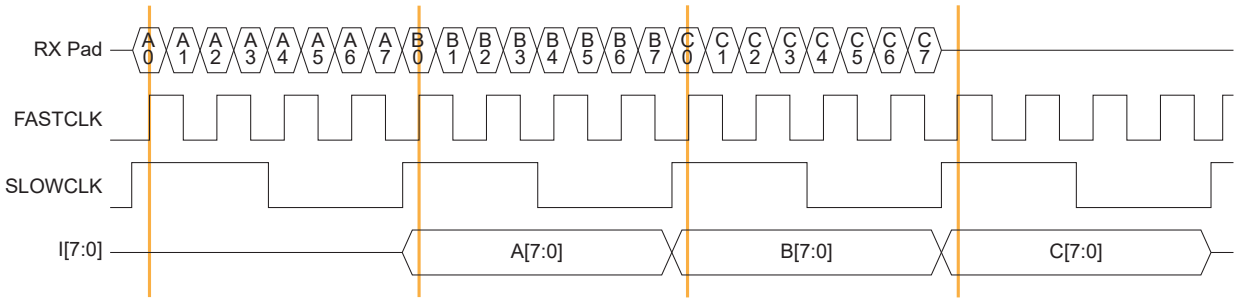
Table 21: LVDS RX Pads

Pad	Direction	Description
RXP	Input	Differential P pad.
RXN	Input	Differential N pad.

Note: You need an external DC-biased circuit if the incoming LVDS signals are AC-coupled. Refer to **Trion Hardware Design Checklist and Guidelines** for more information.

The following waveform shows the relationship between the fast clock, slow clock, RX data coming in from the pad, and byte-aligned data to the core.

Figure 17: LVDS RX Timing Example Serialization Width of 8



I is byte-aligned data passed to the core on the rising edge of SLOWCLK.

Note: For LVDS RX interfaces with multiple LVDS RX lanes and an LVDS RX clock input, use the LVDS RX blocks from the same side of the FPGA to minimize skew between data lanes and RX clock input.

Table 22: LVDS RX Settings in Efinity® Interface Designer

Parameter	Choices	Notes
Instance Name	User defined	
LVDS Resource	Resource list	Choose a resource.
Connection Type	normal, pll_clkin	**normal**—Regular RX function. **pll_clkin**—Use the PLL CLKIN alternate function of the LVDS RX resource.
Input Pin/Bus Name	User defined	Input pin or bus that feeds the LVDS transmitter parallel data. The width should match the deserialization factor.
Enable Deserialization	On or off	When off, the de-serializer is bypassed and the LVDS buffer is used as a normal input. Specify the serial clock and parallel clock.
Deserialization Width	2, 3, 4, 5, 6, 7, or 8	Supports 8:1, 7:1, 6:1, 5:1, 4:1, 3:1, and 2:1.
Enable On-Die Termination	On or off	When on, enables an on-die 100-ohm resistor.
Static Mode Delay Setting	0 - 63	Choose the amount of static delay, each step adds approximately 25 ps of delay.

MIPI

The MIPI CSI-2 interface is the most widely used camera interface for mobile.[7]. You can use this interface to build single- or multi-camera designs for a variety of applications.

T13 FPGAs include two hardened MIPI D-PHY blocks (4 data lanes and 1 clock lane) with MIPI CSI-2 IP blocks. The MIPI RX and MIPI TX can operate independently with dedicated I/O banks.

Note: The MIPI D-PHY and CSI-2 controller are hard blocks; users cannot bypass the CSI-2 controller to access the D-PHY directly for non-CSI-2 applications.

The MIPI TX/RX interface supports the MIPI CSI-2 specification v1.3 and the MIPI D-PHY specification v1.1. It has the following features:

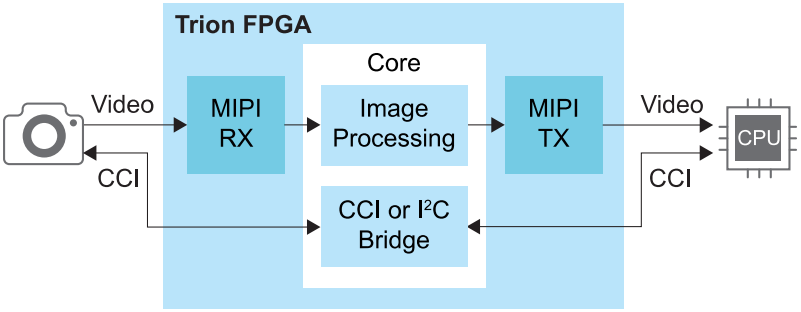
- Programmable data lane configuration supporting 1, 2, or 4 lanes
- High-speed mode supports up to 1.5 Gbps data rates per lane
- Operates in continuous and non-continuous clock modes
- 64 bit pixel interface for cameras
- Supports Ultra-Low Power State (ULPS)

Table 23: MIPI Supported Data Types

Supported Data Type	Format
RAW	RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
YUV	YUV420 8-bit (legacy), YUV420 8-bit, YUV420 10-bit, YUV420 8-bit (CSPS), YUV420 10-bit (CSPS), YUV422 8-bit, YUV422 10-bit
RGB	RGB444, RGB555, RGB565, RGB666, RGB888
User Defined	8 bit format

With more than one MIPI TX and RX blocks, Trion® FPGAs support a variety of video applications.

Figure 18: MIPI Example System

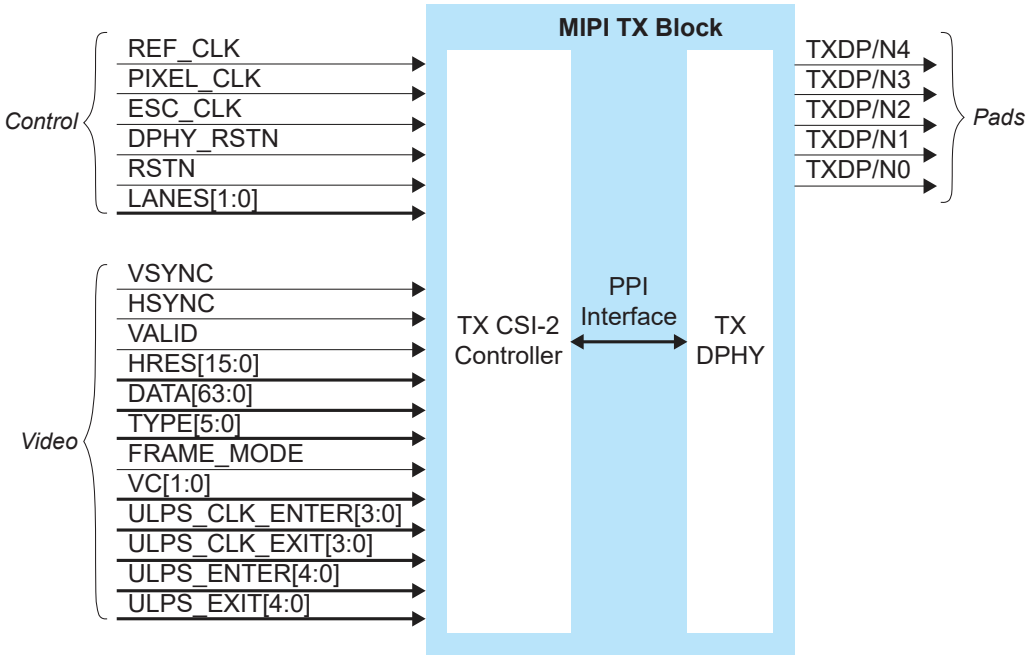


MIPI TX

The MIPI TX is a transmitter interface that translates video data from the Trion® core into packetized data sent over the HSSI interface to the board. Five high-speed differential pin pairs (four data, one clock), each of which represent a lane, connect to the board. Control and video signals connect from the MIPI interface to the core.

[7] Source: MIPI Alliance **https://www.mipi.org/specifications/csi-2**

Figure 19: MIPI TX x4 Block Diagram



The control signals determine the clocking and how many transceiver lanes are used. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The MIPI block requires an escape clock (`ESC_CLK`) for use when the MIPI interface is in escape (low-power) mode, which runs between 11 and 20 MHz.

Note: Elitestek recommends that you set the escape clock frequency as close to 20 MHz as possible.

The video signals receive the video data from the core. The MIPI interface block encodes is and sends it out through the MIPI D-PHY lanes.

Figure 20: MIPI TX Interface Block Diagram

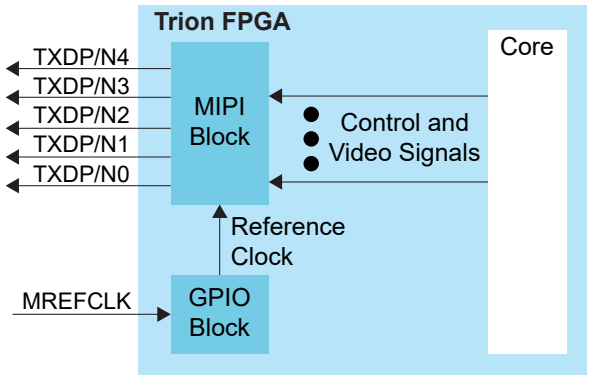


Table 24: MIPI TX Control Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
REF_CLK	Input	N/A	Reference clock for the internal MIPI TX PLL used to generate the transmitted data. The FPGA has a dedicated GPIO resource (MREFCLK) that you must configure to provide the reference clock. All of the MIPI TX blocks share this resource. The frequency is set using Interface Designer configuration options.
PIXEL_CLK	Input	N/A	Clock used for transferring data from the core to the MIPI TX block. The frequency is based on the number of lanes and video format.

Signal	Direction	Clock Domain	Description
ESC_CLK	Input	N/A	Slow clock for escape mode (11 - 20 MHz).
DPHY_RSTN	Input	N/A	(Optional) Reset for the D-PHY logic, active low. Reset with the controller. See **MIPI Reset Timing**.
RSTN	Input	N/A	(Optional) Reset for the CSI-2 controller logic, active low. Typically, you reset the controller with the PHY. (See **MIPI Reset Timing**.) However, when dynamically changing the horizontal resolution, you only need to trigger RSTN. (See **TX Requirements for Dynamically Changing the Horizontal Resolution**).
LANES[1:0]	Input	PIXEL_CLK	Determines the number of lanes enabled. Can only be changed during reset. 00: lane 0 01: lanes 0 and 1 11: all lanes

Table 25: MIPI TX Video Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Description
VSYNC	Input	PIXEL_CLK	Vertical sync.
HSYNC	Input	PIXEL_CLK	Horizontal sync.
VALID	Input	PIXEL_CLK	Valid signal.
HRES[15:0]	Input	PIXEL_CLK	Horizontal resolution. Can only be changed when VSYNC is low, and should be stable for at least one TX pixel clock cycle before VSYNC goes high.
DATA[63:0]	Input	PIXEL_CLK	Video data; the format depends on the data type. New data arrives on every pixel clock.
TYPE[5:0]	Input	PIXEL_CLK	Video data type. Can only be changed when HSYNC is low, and should be stable for at least one TX pixel clock cycle before HSYNC goes high.
FRAME_MODE	Input	PIXEL_CLK	Selects frame format. [8] 0: general frame 1: accurate frame Can only be changed during reset.
VC[1:0]	Input	PIXEL_CLK	Virtual channel (VC). Can only be changed when VSYNC is low, and should be stable at least one TX pixel clock cycle before VSYNC goes high.
ULPS_CLK_ENTER	Input	PIXEL_CLK	Place the clock lane into ULPS mode. Should not be active at the same time as ULPS_CLK_EXIT. Each high pulse should be at least 5 µs.
ULPS_CLK_EXIT	Input	PIXEL_CLK	Remove clock lane from ULPS mode. Should not be active at the same time as ULPS_CLK_ENTER. Each high pulse should be at least 5 µs.
ULPS_ENTER[3:0]	Input	PIXEL_CLK	Place the data lane into ULPS mode. Should not be active at the same time as ULPS_EXIT[3:0]. Each high pulse should be at least 5 µs.
ULPS_EXIT[3:0]	Input	PIXEL_CLK	Remove the data lane from ULPS mode. Should not be active at the same time as ULPS_ENTER[3:0]. Each high pulse should be at least 5 µs.

Table 26: MIPI TX Pads

Pad	Direction	Description
TXDP[4:0]	Output	MIPI transceiver P pads.
TXDN[4:0]	Output	MIPI transceiver N pads.

[8] Refer to the MIPI Camera Serial Interface 2 (MIPI CSI-2) for more information about frame formats.

Table 27: MIPI TX Settings in Efinity® Interface Designer

Tab	Parameter	Choices	Notes
Base	PHY Bandwidth (Mbps)	80.00 - 1500.00	Choose one of the possible PHY bandwidth values.
	Frequency (reference clock)	6, 12, 19.2, 25, 26, 27, 38.4, or 52 MHz	Reference clock frequency.
	Enable Continuous PHY Clocking	On or Off	Turns continuous clock mode on or off.
Control	Escape Clock Pin Name	User defined	
	Invert Escape Clock	On or Off	
	Pixel Clock Pin Name	User defined	
	Invert Pixel Clock	On or Off	
Lane Mapping	TXD0, TXD1, TXD2, TXD3, TXD4	clk, data0, data1, data2, or data3	Map the physical lane to a clock or data lane.
	Clock Timer		
Timing	$T_{CLK-POST}$ $T_{CLK-TRAIL}$ $T_{CLK-PREPARE}$ $T_{CLK-ZERO}$	Varies depending on the PHY frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to **D-PHY Timing Parameters** on page 35.
	Escape Clock Frequency (MHz)	User defined	Specify a number between 11 and 20 MHz.
	$T_{CLK-PRE}$	Varies depending on the escape clock frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to **D-PHY Timing Parameters** on page 35.
	Data Timer		
	$T_{HS-PREPARE}$ $T_{HS-ZERO}$ $T_{HS-PTRAIL}$	Varies depending on the PHY frequency	Changes the MIPI transmitter timing parameters per the DPHY specification. Refer to **D-PHY Timing Parameters** on page 35.

MIPI TX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

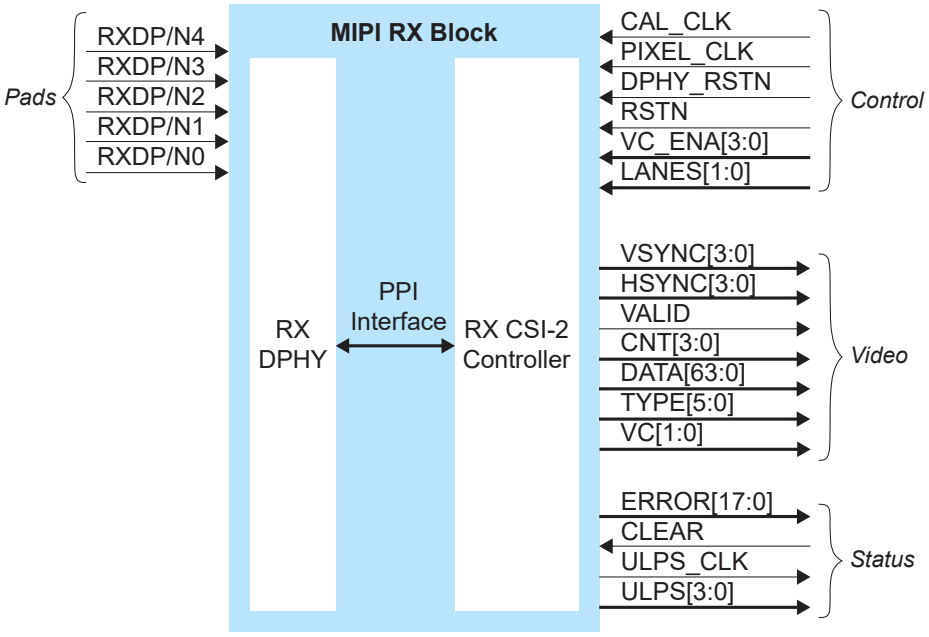
Table 28: MIPI TX TYPE[5:0]

TYPE[5:0]	Data Type	Pixel Data Bits per Pixel Clock	Pixels per Clock	Bits per Pixel	Maximum Data Pixels per Line
0x20	RGB444	48	4	12	2,880
0x21	RGB555	60	4	15	2,880
0x22	RGB565	64	4	16	2,880
0x23	RGB666	54	3	18	2,556
0x24	RGB888	48	2	24	1,920
0x28	RAW6	60	10	6	7,680
0x29	RAW7	56	8	7	6,576
0x2A	RAW8	64	8	8	5,760
0x2B	RAW10	60	6	10	4,608
0x2C	RAW12	60	5	12	3,840
0x2D	RAW14	56	4	14	3,288
0x18	YUV420 8 bit	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x19	YUV420 10 bit	Odd line: 60 Even line: 40	Odd line: 6 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1A	Legacy YUV420 8 bit	48	4	8, 16	3,840
0x1C	YUV420 8 bit (CSPS)	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x1D	YUV420 10 bit (CSPS)	Odd line: 60 Even line: 40	Odd line: 6 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1E	YUV422 8 bit	64	4	8, 24	2,880
0x1F	YUV422 10 bit	40	2	10, 30	2,304
0x30 - 37	User defined 8 bit	64	8	8	5,760

MIPI RX

The MIPI RX is a receiver interface that translates HSSI signals from the board to video data in the Trion® core. Five high-speed differential pin pairs (one clock, four data), each of which represent a lane, connect to the board. Control, video, and status signals connect from the MIPI interface to the core.

Figure 21: MIPI RX x4 Block Diagram



The control signals determine the clocking, how many transceiver lanes are used, and how many virtual channels are enabled. All control signals are required except the two reset signals. The reset signals are optional, however, you must use both signals or neither.

The video signals send the decoded video data to the core. All video signals must fully support the MIPI standard.

The status signals provide optional status and error information about the MIPI RX interface operation.

Figure 22: MIPI RX Interface Block Diagram

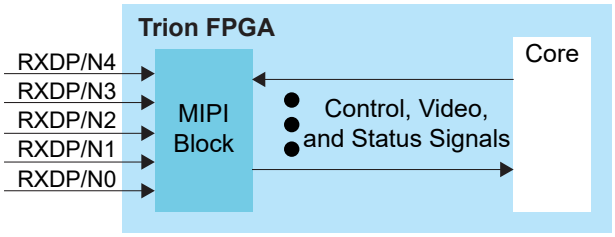


Table 29: MIPI RX Control Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
CAL_CLK	Input	N/A	Used for D-PHY calibration; must be between 80 and 120 MHz.
PIXEL_CLK	Input	N/A	Clock used for transferring data to the core from the MIPI RX block. The frequency based on the number of lanes and video format.
DPHY_RSTN	Input	N/A	(Optional) Reset for the D-PHY logic, active low. Must be used if RSTN is used. See **MIPI Reset Timing**.
RSTN	Input	N/A	(Optional) Reset for the CSI-2 controller logic, active low. Must be used if DPHY_RSTN is used. See **MIPI Reset Timing**.
VC_ENA[3:0]	Input	PIXEL_CLK	Enables different VC channels by setting their index high.
LANES[1:0]	Input	PIXEL_CLK	Determines the number of lanes enabled: 00: lane 0 01: lanes 0 and 1 11: all lanes Can only be set during reset.

Table 30: MIPI RX Video Signals (Interface to FPGA Fabric)

Signal	Direction	Clock Domain	Notes
VSYNC[3:0]	Output	PIXEL_CLK	Vsync bus. High if vsync is active for this VC.
HSYNC[3:0]	Output	PIXEL_CLK	Hsync bus. High if hsync is active for this VC
VALID	Output	PIXEL_CLK	Valid signal.
CNT[3:0]	Output	PIXEL_CLK	Number of valid pixels contained in the pixel data.
DATA[63:0]	Output	PIXEL_CLK	Video data, format depends on data type. New data every pixel clock.
TYPE[5:0]	Output	PIXEL_CLK	Video data type.
VC[1:0]	Output	PIXEL_CLK	Virtual channel (VC).

Table 31: MIPI RX Status Signals (Interface to FPGA Fabric)

Signal	Direction	Signal Interface	Clock Domain	Notes
ERROR[17:0]	Output	IN	PIXEL_CLK	Error bus register. Refer to **Table 32: MIPI RX Error Signals (ERROR[17:0])** on page 32 for details.
CLEAR	Input	OUT	PIXEL_CLK	Reset the error registers.
ULPS_CLK	Output	IN	PIXEL_CLK	High when the clock lane is in the Ultra-Low-Power State (ULPS).
ULPS[3:0]	Output	IN	PIXEL_CLK	High when the lane is in the ULPS mode.

Table 32: MIPI RX Error Signals (ERROR[17:0])

Bit	Name	Description
0	ERR_ESC	Escape Entry Error. Asserted when an unrecognized escape entry command is received.
1	CRC_ERROR_VC0	CRC Error VC0. Set to 1 when a checksum error occurs.
2	CRC_ERROR_VC1	CRC Error VC1. Set to 1 when a checksum error occurs.
3	CRC_ERROR_VC2	CRC Error VC2. Set to 1 when a checksum error occurs.
4	CRC_ERROR_VC3	CRC Error VC3. Set to 1 when a checksum error occurs.
5	HS_RX_TIMEOUT_ERR	HS RX Timeout Error. The protocol should time out when no EoT is received within a certain period in HS RX mode.
6	ECC_1BIT_ERROR	ECC Single Bit Error. Set to 1 when there is a single bit error.
7	ECC_2BIT_ERROR	ECC 2 Bit Error. Set to 1 if there is a 2 bit error in the packet.
8	ECCBIT_ERROR	ECC Error. Asserted when an error exists in the ECC.
9	ECC_NO_ERROR	ECC No Error. Asserted when an ECC is computed with a result zero. This bit is high when the receiver is receiving data correctly.
10	FRAME_SYNC_ERROR	Frame Sync Error. Asserted when a frame end is not paired with a frame start on the same virtual channel.
11	INVLD_PKT_LEN	Invalid Packet Length. Set to 1 if there is an invalid packet length.
12	INVLD_VC	Invalid VC ID. Set to 1 if there is an invalid CSI VC ID.
13	INVALID_DATA_TYPE	Invalid Data Type. Set to 1 if the received data is invalid.
14	ERR_FRAME	Error In Frame. Asserted when VSYNC END received when CRC error is present in the data packet.
15	CONTROL_ERR	Control Error. Asserted when an incorrect line state sequence is detected.
16	SOT_ERR	Start-of-Transmission (SoT) Error. Corrupted high-speed SoT leader sequence while proper synchronization can still be achieved.
17	SOT_SYNC_ERR	SoT Synchronization Error. Corrupted high-speed SoT leader sequence while proper synchronization cannot be expected.



Note: If error report is all logic low, there is an EOT or a contention error. Check the physical connection of MIPI lanes or adjust the EXIT and TRAIL parameters according to the MIPI Utility.

Table 33: MIPI RX Pads

Pad	Direction	Description
RXDP[4:0]	Input	MIPI transceiver P pads.
RXDN[4:0]	Input	MIPI transceiver N pads.

Table 34: MIPI RX Settings in Efinity® Interface Designer

Tab	Parameter	Choices	Notes
Control	DPHY Calibration Clock Pin Name	User defined	
	Invert DPHY Calibration Clock	On or Off	
	Pixel Clock Pin Name	User defined	
	Invert Pixel Clock	On or Off	
Status	Enable Status	On or Off	Indicate whether you want to use the status pins.
Lane Mapping	RXD0, RXD1, RXD2, RXD3, RXD4	clk, data0, data1, data2, or data3	Map the physical lane to a clock or data lane.
	Swap P&N Pin	On or Off	Reverse the P and N pins for the physical lane.
Timing	Calibration Clock Freq (MHz)	User defined	Specify a number between 80 and 120 MHz.
	Clock Timer ($T_{CLK-SETTLE}$)	40 - 2,590 ns	Changes the MIPI receiver timing parameters per the DPHY specification. Refer to **D-PHY Timing Parameters** on page 35.
	Data Timer ($T_{HS-SETTLE}$)	40 - 2,590 ns	Changes the MIPI receiver timing parameters per the DPHY specification. Refer to **D-PHY Timing Parameters** on page 35.

MIPI RX Video Data TYPE[5:0] Settings

The video data type can only be changed when HSYNC is low.

Table 35: MIPI RX TYPE[5:0]

TYPE[5:0]	Data Type	Pixel Data Bits per Pixel Clock	Pixels per Clock	Bits per Pixel	Maximum Data Pixels per Line
0x20	RGB444	48	4	12	2,880
0x21	RGB555	60	4	15	2,880
0x22	RGB565	64	4	16	2,880
0x23	RGB666	54	3	18	2,556
0x24	RGB888	48	2	24	1,920
0x28	RAW6	48	8	6	7,680
0x29	RAW7	56	8	7	6,576
0x2A	RAW8	64	8	8	5,760
0x2B	RAW10	40	4	10	4,608
0x2C	RAW12	48	4	12	3,840
0x2D	RAW14	56	4	14	3,288
0x18	YUV420 8 bit	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x19	YUV420 10 bit	Odd line: 40 Even line: 40	Odd line: 4 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1A	Legacy YUV420 8 bit	48	4	8, 16	3,840
0x1C	YUV420 8 bit (CSPS)	Odd line: 64 Even line: 64	Odd line: 8 Even line: 4	Odd line: 8 Even line: 8, 24	2,880
0x1D	YUV420 10 bit (CSPS)	Odd line: 40 Even line: 40	Odd line: 4 Even line: 2	Odd line: 10 Even line: 10, 30	2,304
0x1E	YUV422 8 bit	64	4	8, 24	2,880
0x1F	YUV422 10 bit	40	2	10, 30	2,304
0x30 - 37	User defined 8 bit	64	8	8	5,760

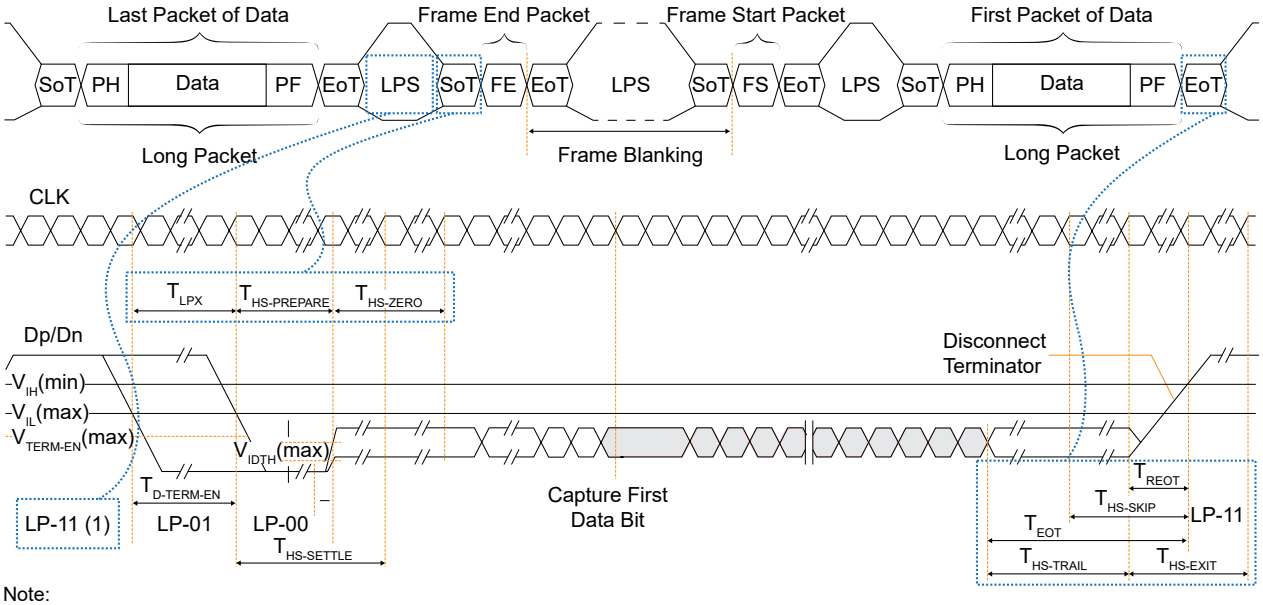
D-PHY Timing Parameters

During CSI-2 data transmission, the MIPI D-PHY alternates between low power mode and high-speed mode. The D-PHY specification defines timing parameters to facilitate the correct hand-shaking between the MIPI TX and MIPI RX during mode transitions.

You set the timing parameters to correspond to the specifications of your hardware in the Efinity® Interface Designer.

- *RX parameters*—$T_{CLK-SETTLE}$, $T_{HS-SETTLE}$ (see **Table 29: MIPI RX Control Signals (Interface to FPGA Fabric)** on page 31)
- *TX parameters*—$T_{CLK-POST}$, $T_{CLK-TRAIL}$, $T_{CLK-PREPARE}$, $T_{CLK-ZERO}$, $T_{CLK-PRE}$, $T_{HS-PREPARE}$, $T_{HS-ZERO}$, $T_{HS-TRAIL}$ (see **Table 27: MIPI TX Settings in Efinity Interface Designer** on page 28)

Figure 23: High-Speed Data Transmission in Bursts Waveform



Note:
1. To enter high-speed mode, the D-PHY goes through states LP-11, LP-01, and LP-00. The D-PHY generates LP-11 to exit high-speed mode.

Figure 24: Switching the Clock Lane between Clock Transmission and Low Power Mode Waveform

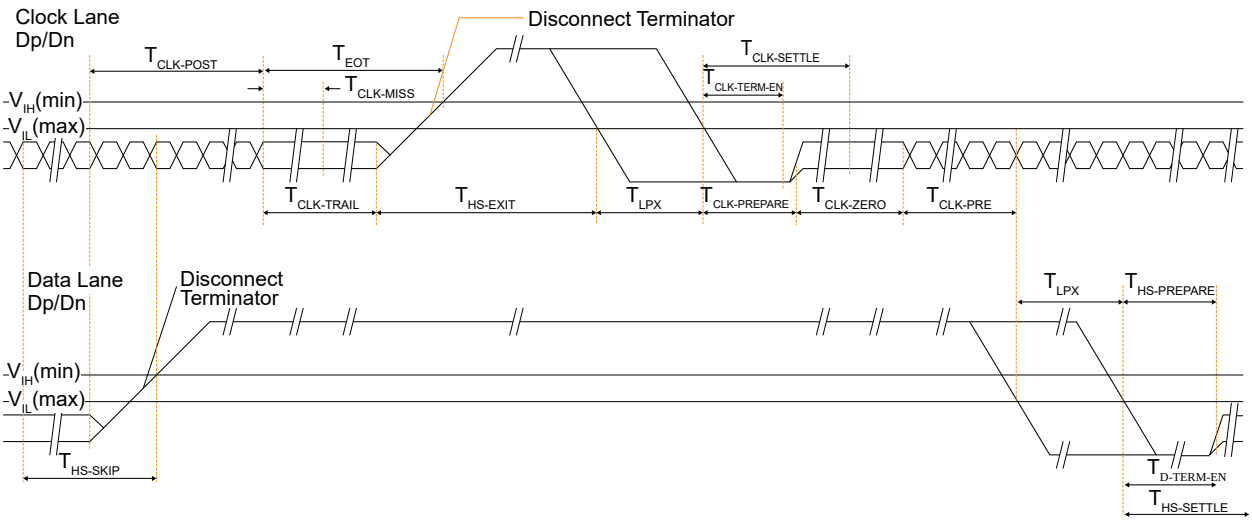


Table 36: D-PHY Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI	–	–	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	–	–	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38	–	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$.	95	–	300	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60	–	–	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock.	300	–	–	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI	–	85 ns + 6*UI	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85 ns + 6*UI	–	145 ns + 10*UI	ns
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.	max(*n**8*UI, 60 ns + *n**4*UI)[9]	–	–	ns
T_{LPX}	Transmitted length of any Low-Power state period	50	–	–	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI	–	–	ns

[9] Where *n* = 1 in Forward-direction HS mode and *n* = 4 for Reverse-direction HS mode.

SPI Flash Memory

The QFP100F3 packages include a T13 FPGA and a SPI flash memory. The SPI flash memory has a density of 16 Mbits and a clock rate of up to 20 MHz. In active configuration mode, the FPGA is configured using the configuration bitstream in the SPI flash memory. Typically you can fit two compressed bitstream images into the QFP100F3 SPI flash.
The SPI flash memory's VCC is powered by `VCCIO1A_1B_1C` (3.3 V).

When a configuration bitstream is stored in the SPI flash and the SPI active hardware connection is properly established, the SPI active configuration can automatically start after the power-up. In QFP100F3 packages you are only required to connect the `SS_N` pin to the `SPI_CS_N` pin for the SPI active configuration to start automatically. This is additional to other required configuration pin settings depending on the configuration mode you select.

Learn more: Refer to the AN 006: Configuring Trion FPGAs for detailed configuration requirements.

You can also use the SPI flash to store user data during user mode. To read or write the SPI flash during user mode, you must create the SPI flash interface block in the Efinity Interface Designer.

Learn more: Refer to Trion Interfaces User Guide for more information about using the SPI flash interface block in the Efinity Interface Designer.

Important: You can only use the internal SPI flash in user mode if no LVDS TX is used.

Figure 25: SPI Flash Memory Block Diagram

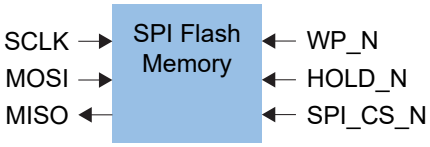


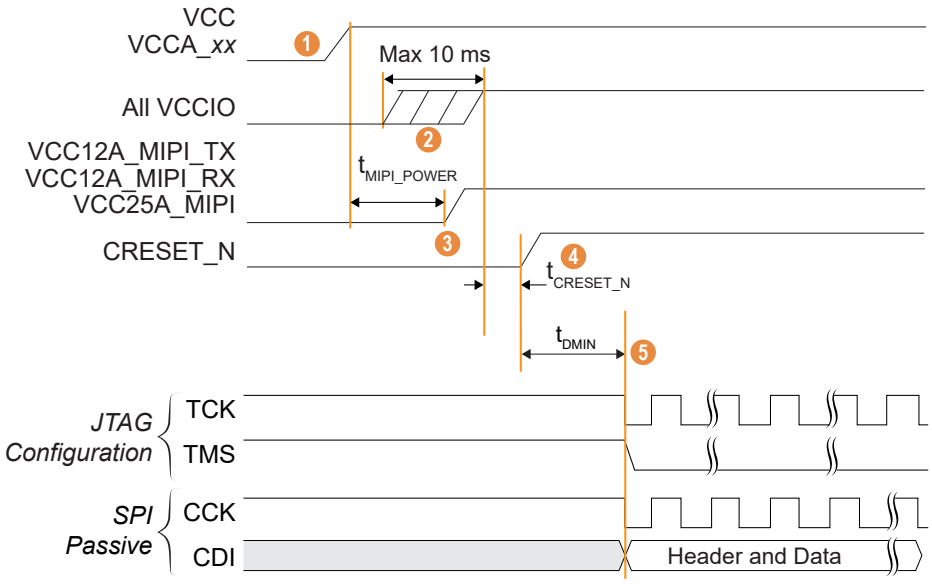
Table 37: SPI Flash Memory Signals (Interface to FPGA Fabric)

Signal	Direction	Description
SCLK	Input	Clock output to SPI flash memory.
MOSI	Input	Data output to SPI flash memory.
MISO	Output	Data input from SPI flash memory.
WP_N	Input	Active-low write protect signal.
HOLD_N	Input	Active-low hold signal.
SPI_CS_N	Input	Active-low SPI flash memory chip select.

Power Up Sequence

Elitestek® recommends the following power up sequence when powering Trion® FPGAs:

Figure 26: Trion® FPGAs Power Up Sequence



1. Power up `VCC` and `VCCA_xx` first.
2. When `VCC` and `VCCA_xx` are stable, power up all VCCIO pins. There is no specific timing delay between the VCCIO pins.
3. Apply power to `VCC12A_MIPI_TX`, `VCC12A_MIPI_RX`, and `VCC25A_MIPI` at least t_{MIPI_POWER} after `VCC` is stable.

   Important: Ensure the power ramp rate is within VCCIO/10 V/ms to 10 V/ms.

4. After all power supplies are stable, hold `CRESET_N` low for a duration of t_{CRESET_N} before asserting `CRESET_N` from low to high to trigger active SPI programming (the FPGA loads the configuration data from an external flash device).
5. FPGA configuration can begin after there has been a t_{DMIN} minimum delay after `CRESET_N` goes high (see **SPI Passive** and **JTAG** for the delay specification).

When you are not using the GPIO, MIPI or PLL resources, connect the pins as shown in the following table.

Note: Refer to **Configuration Timing** on page 54 and **MIPI Power-Up Timing** on page 50 for timing information.

Power Supply Current Transient

You may observe an inrush current on the dedicated power rail during power-up. You must ensure that the power supplies selected in your board meets the current requirement during power-up and the estimated current during user mode. Use the Power Estimator to calculate the estimated current during user mode.

Table 38: Maximum Power Supply Current Transient

Power Supply	Maximum Power Supply Current Transient[10][11]	Unit
VCC	35	mA

Unused Resources and Features

Table 39: Connection Requirements for Unused Resources

Unused Resource	Pin	Note
GPIO Bank	VCCIOxx	Connect to either 1.8 V, 2.5 V, or 3.3 V.
PLL	VCCA_PLL	Connect to VCC (1.2 V).
MIPI	VCC12A_MIPI_TX	Connect to VCC (1.2 V).
	VCC12A_MIPI_RX	Connect to VCC (1.2 V).
	VCC25A_MIPI	Connect to VCC (1.2 V).

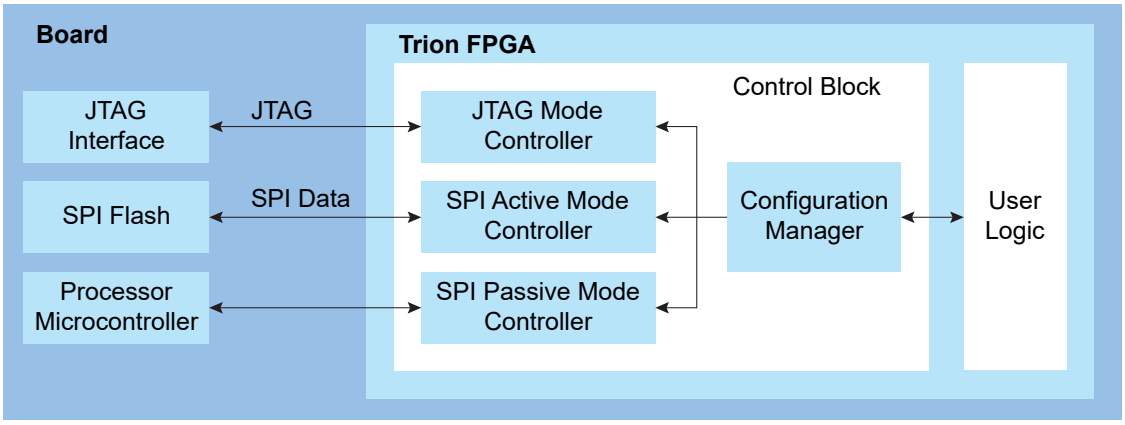
(10) Inrush current for other power rails are not significant in Trion® FPGAs.
(11) Measured at room temperature.

Configuration

The T13 FPGA contains volatile Configuration RAM (CRAM). The user must configure the CRAM for the desired logic function upon power-up and before the FPGA enters normal operation. The FPGA's control block manages the configuration process and uses a bitstream to program the CRAM. The Efinity® software generates the bitstream, which is design dependent. You can configure the T13 FPGA(s) in SPI active, SPI passive, or JTAG mode.

Learn more: Refer to AN 006: Configuring Trion FPGAs for details on the dedicated configuration pins and how to configure FPGA(s).

Figure 27: High-Level Configuration Options



In active mode, the FPGA controls the configuration process. An oscillator circuit within the FPGA provides the configuration clock. The bitstream is typically stored in an external serial flash device, which provides the bitstream when the FPGA requests it.

The control block sends out the instruction and address to read the configuration data. First, it issues a release from power-down instruction to wake up the external SPI flash. Then, it waits for at least 30 µs before issuing a fast read command to read the content of SPI flash from address 24h'000000.

In passive mode, the FPGA is the slave and relies on an external master to provide the control, bitstream, and clock for configuration. Typically the master is a microcontroller or another FPGA in active mode.

In JTAG mode, you configure the FPGA via the JTAG interface.

Supported Configuration Modes

Table 40: T13 Configuration Modes by Package

Configuration Mode	Width	Q100F3	F256	F169
Active	x1	✓	✓	✓
	x2	✓	✓	✓
	x4	✓	✓	✓
Passive	x1	✓	✓	✓
	x2	✓	✓	✓
	x4	✓	✓	✓
	x8	✓	✓	
	x16	✓	✓	
	x32		✓	
JTAG	x1	✓	✓	✓

Learn more: Refer to AN 006: Configuring Trion FPGAs for more information.

Mask-Programmable Memory Option

The T13 FPGA is equipped with one-time programmable MPM. With this feature, you use on-chip MPM instead of an external serial flash device to configure the FPGA. This option is for systems that require an ultra-small factor and the lowest cost structure such that an external serial flash device is undesirable and/or not required at volume production. MPM is a one-time factory programmable option that requires a Non-Recurring Engineering (NRE) payment. To enable MPM, submit your design to our factory; our Applications Engineers (AEs) convert your design into a single configuration mask to be specially fabricated.

DC and Switching Characteristics

Table 41: Absolute Maximum Ratings

Conditions beyond those listed may cause permanent damage to the device. Device operation at the absolute maximum ratings for extended periods of time has adverse effects on the device.

Symbol	Description	Min	Max	Units
VCC	Core power supply	-0.5	1.42	V
VCCIO	I/O bank power supply	-0.5	4.6	V
	I/O bank 1A_1B_1C power supply (QFP100F3)	-0.5	4.1	V
VCCA_PLL	PLL analog power supply	-0.5	1.42	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	-0.5	2.75	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	-0.5	1.42	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	-0.5	1.42	V
V_{IN}	I/O input voltage	-0.5	4.6	V
I_{IN}	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.(13)	–	10	mA
T_J	Operating junction temperature	-40	125	°C
	Operating junction temperature (QFP100F3)	-40	105	°C
T_{STG}	Storage temperature, ambient	-55	150	°C

(12) Supply voltage specification applied to the voltage taken at the device pins with respect to ground, not at the power supply.
(13) Should not exceed a total of 120 mA per bank.

Table 42: Recommended Operating Conditions (C3, C4, Q4, and I4 Speed Grades) [12]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.15	1.2	1.25	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.15	1.2	1.25	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	2.38	2.5	2.63	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.2 V TX analog power supply for MIPI	1.15	1.2	1.25	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.2 V RX analog power supply for MIPI	1.15	1.2	1.25	V
V_{IN}	I/O input voltage[14]	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C
T_{JAUT}	Operating junction temperature, automotive	-40	–	105	°C

Table 43: Recommended Operating Conditions (C4L and I4L Speed Grades) [12]

Symbol	Description	Min	Typ	Max	Units
VCC	Core power supply	1.05	1.1	1.15	V
VCCIO	1.8 V I/O bank power supply	1.71	1.8	1.89	V
	2.5 V I/O bank power supply	2.38	2.5	2.63	V
	3.3 V I/O bank power supply	3.14	3.3	3.47	V
VCCA_PLL	PLL analog power supply	1.05	1.1	1.15	V
VCC25A_MIPI0 VCC25A_MIPI1	2.5 V analog power supply for MIPI	2.38	2.5	2.63	V
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	1.1 V TX analog power supply for MIPI	1.05	1.1	1.15	V
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	1.1 V RX analog power supply for MIPI	1.05	1.1	1.15	V
V_{IN}	I/O input voltage[15]	-0.3	–	VCCIO + 0.3	V
T_{JCOM}	Operating junction temperature, commercial	0	–	85	°C
T_{JIND}	Operating junction temperature, industrial	-40	–	100	°C

[14] Values applicable to both input and tri-stated output configuration.
[15] Values applicable to both input and tri-stated output configuration.

Table 44: Power Supply Ramp Rates

Symbol	Description	Min	Max	Units
t_{RAMP}	Power supply ramp rate for all supplies.	VCCIO/10	10	V/ms

Table 45: Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4
2.5 V LVCMOS	-0.3	0.7	1.7	VCCIO + 0.3	0.5	1.8
1.8 V LVCMOS	-0.3	0.35 * VCCIO	0.65 * VCCIO	VCCIO + 0.3	0.45	VCCIO - 0.45

Table 46: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic

Voltage (V)	VT+ (V) Schmitt Trigger Low-to-High Threshold	VT- (V) Schmitt Trigger High-to-Low Threshold	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	1.73	1.32	±10	±10
2.5	1.37	1.01	±10	±10
1.8	1.05	0.71	±10	±10

Table 47: Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at T_J = 25 °C, power supply at nominal voltage.

CDONE has a drive strength of 1.

I/O Standard	3.3 V		2.5 V		1.8 V	
Drive Strength	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)	I_{OH} (mA)	I_{OL} (mA)
1	14.4	8.0	9.1	8.0	5.1	4.4
2	19.1	10.5	12.2	10.5	6.8	5.8
3	23.9	13.3	15.2	13.4	8.6	7.3
4	28.7	15.8	18.2	15.9	10.3	8.6

Table 48: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance

CDONE and CRESET_N also have an internal weak pull-up with these values.

I/O Standard	Internal Pull-Up			Internal Pull-Down			Units
	Min	Typ	Max	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	30	47	83	kΩ
2.5 V LVCMOS	35	55	120	37	62	118	kΩ
1.8 V LVCMOS	70	90	200	80	99	300	kΩ

Table 49: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

I/O Standard	V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)
	Min	Max	Min	Max	Max	Min
3.3 V LVCMOS	-0.3	0.8	2	VCCIO + 0.3	0.2	VCCIO - 0.2
3.3 V LVTTL	-0.3	0.8	2	VCCIO + 0.3	0.4	2.4

Table 50: LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics

Junction temperature at TJ = 25 °C, power supply at nominal voltage, device in nominal process (TT).

I/O Standard	Drive Strength	
	I_{OH}(mA)	I_{OL}(mA)
3.3 V	37.6	22

Table 51: LVDS Pins Configured as Single-Ended I/O DC Electrical Characteristics

Voltage (V)	Input Leakage Current (µA)	Tri-State Output Leakage Current (µA)
3.3	±10	±10

Table 52: LVDS Pins Configured as Single-Ended I/O Internal Weak Pull-Up Resistance

I/O Standard	Internal Pull-Up			Units
	Min	Typ	Max	
3.3 V LVTTL/LVCMOS	27	40	65	kΩ

Table 53: Maximum Toggle Rate

Elitestek recommends that you perform simulations using the IBIS model to determine the maximum toggle rate for your design.

I/O Standard	Package	Max Toggle Rate	Units
3.3 V LVTTL/LVCMOS	All	400	Mbps
2.5 V LVCMOS	All	400	Mbps
1.8 V LVCMOS	All	400	Mbps
LVDS	All others	800	Mbps
	QFP100F3	600	Mbps

Table 54: Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time

Data are based on the following IBIS simulation setup:

- Weakest drive strength model
- Typical simulation corner setting
- RLC circuit with 6.6 pF capacitance, 16.6 nH inductance, 0.095 ohm resistance, and 25 °C temperature

Note: For a more accurate data, you need to perform the simulation with your own circuit.

I/O Standard	Rise Time (T_R)		Fall Time (T_F)		Units
	Slow Slew Rate Enabled	Slow Slew Rate Disabled	Slow Slew Rate Enabled	Slow Slew Rate Disabled	
3.3 V LVTTL/LVCMOS	1.13	1.02	1.24	1.17	ns
2.5 V LVCMOS	1.4	1.3	1.44	1.31	ns
1.8 V LVCMOS	2.14	2.01	2.05	1.85	ns
LVDS pins configured as 3.3 V LVTTL/ LVCMOS	0.45		0.44		ns

Table 55: Block RAM Characteristics

Symbol	Description	Speed Grade		Units
		C3, C4L, I4L	C4, I4, Q4	
f_{MAX}	Block RAM maximum frequency.	310	400	MHz

Table 56: Multiplier Block Characteristics

Symbol	Description	Speed Grade		Units
		C3, C4L, I4L	C4, I4, Q4	
f_{MAX}	Multiplier block maximum frequency.	310	400	MHz

LVDS I/O Electrical and Timing Specifications

The LVDS pins comply with the EIA/TIA-644 electrical specifications.

Note: The LVDS RX supports the sub-lvds, slvs, HiVcm, RSDS and 3.3 V LVPECL differential I/O standards with a transfer rate of up to 800 Mbps.

Table 57: LVDS I/O Electrical Specifications

Parameter	Description	Test Conditions/ Options	Min	Typ	Max	Unit
V_{CCIO}	LVDS I/O Supply Voltage	–	2.97	3.3	3.63	V
LVDS TX						
V_{OD}	Output Differential Voltage	Reduce VOD Swing option disabled	250	350	450	mV
		Reduce VOD Swing option enabled	150	200	250	mV
ΔV_{OD}	Change in V_{OD}	–	–	–	50	mV
V_{OCM}	Output Common Mode Voltage	RT = 100 Ω	1,125	1,250	1,375	mV
ΔV_{OCM}	Change in V_{OCM}	–	–	–	50	mV
V_{OH}	Output High Voltage	RT = 100 Ω	–	–	1475	mV
V_{OL}	Output Low Voltage	RT = 100 Ω	925	–	–	mV
I_{SAB}	Output Short Circuit Current	–	–	–	24	mA
LVDS RX						
V_{ID}	Input Differential Voltage	–	100	–	600	mV
V_{ICM}	Input Common Mode Voltage	–	100	–	2,000	mV
V_{TH}	Differential Input Threshold	–	-100	–	100	mV
I_{IL}	Input Leakage Current	–	–	–	20	µA

Figure 28: LVDS RX I/O Electrical Specification Waveform

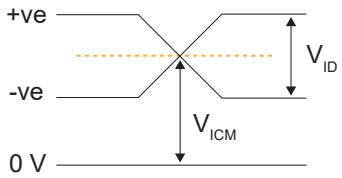


Table 58: LVDS Timing Specifications

Parameter	Description	Min	Typ	Max	Unit
t_{LVDS_CPA}	LVDS TX reference clock phase accuracy	-5	–	+5	%
t_{LVDS_skew}	LVDS TX lane-to-lane skew (edge-aligned)	–	–	200	ps
	LVDS TX lane-to-lane skew (center-aligned)	–	–	250	ps
t_{LVDS_SU}	LVDS RX Data to CLK setup time	344	–	–	ps
t_{LVDS_HD}	LVDS RX Data to CLK hold time	344	–	–	ps

Figure 29: LVDS RX Timing (Center-Aligned)

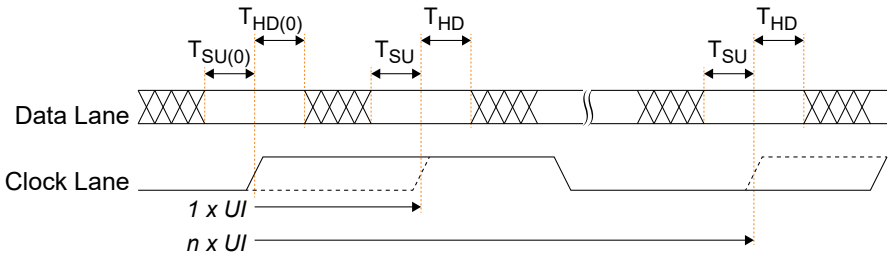
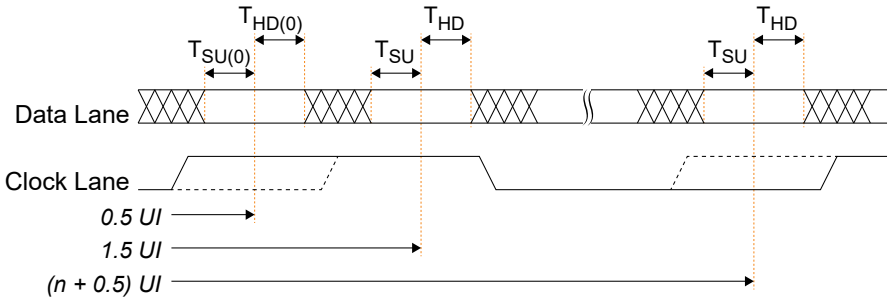


Figure 30: LVDS RX Timing (Edge-Aligned)



ESD Performance

Refer to the Trion Reliability Report for ESD performance data.

MIPI Electrical Specifications and Timing

The MIPI D-PHY transmitter and receiver are compliant to the MIPI Alliance Specification for D-PHY Revision 1.1.

Table 59: High–Speed MIPI D–PHY Transmitter (TX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{CMTX}	High–speed transmit static common–mode voltage	150	200	250	mV
$\|\Delta V_{CMTX(1,0)}\|$	V_{CMTX} mismatch when output is Differential–1 or Differential–0	–	–	5	mV
$\|V_{OD}\|$	High–speed transmit differential voltage	140	200	270	mV
$\|\Delta V_{OD}\|$	VOD mismatch when output is Differential–1 or Differential–0	–	–	14	mV
V_{OHHS}	High–speed output high voltage	–	–	360	mV
Z_{OS}	Single ended output impedance	40	50	60	Ω
ΔZ_{OS}	Single ended output impedance mismatch	–	–	20	%

Table 60: High–Speed MIPI D–PHY Transmitter (TX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	–	–	15	mV_{RMS}
$\Delta V_{CMTX(LF)}$	Common-level variations between 50 to 450 MHz	–	–	25	mV_{PEAK}
t_R and t_F	Rise and fall time < 1.0 Gbps	–	–	0.3	UI
	Rise and fall time > 1.0 Gbps	–	–	0.35	UI
	Rise and fall time > 1.5 Gbps	–	–	0.4	UI

Table 61: Low–Power MIPI D–PHY Transmitter (TX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{OH}	Thevenin output high level	0.95	1.2	1.3	V
V_{OL}	Thevenin output low level	–50	–	50	mV
Z_{OLP}	Output impedance of low–power transmitter	110	–	–	Ω

Table 62: Low-Power MIPI D–PHY Transmitter (TX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}	15%-85% rise time and fall time	–	–	25	ns
T_{REOT}	30%-85% rise time and fall time	–	–	35	ns
$T_{LP-PULSE-TX}$	Pulse width of first LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	–	–	ns
	Pulse width of all other pulses	–	20	–	ns
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock	90	–	–	ns
$\delta V/\delta t_{SR}$	Slew rate at C_{LOAD} = 50 pF < 1.5 Gbps	30	–	150	mV/ns
	Slew rate at C_{LOAD} = 50 pF > 1.5 Gbps	25	–	150	mV/ns

Table 63: High–Speed MIPI D–PHY Receiver (RX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
$V_{CMRX(DC)}$	Common mode voltage high–speed receive mode	70	–	330	mV
Z_{ID}	Differential input impedance	80	100	120	Ω

Table 64: High–Speed MIPI D–PHY Receiver (RX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-point interference above 450 MHz	–	–	50	mV
$\Delta_{VCMRX(LF)}$	Common-point interference between 50 MHz to 450 MHz	–	–	25	mV
V_{IDTH}	Differential input high threshold	–	–	40	mV
V_{IDTL}	Differential input low threshold	–40	–	–	mV
V_{IHHS}	Single–ended input high voltage	–	–	460	mV
V_{ILHS}	Single–ended input low voltage	–40	–	–	mV
$V_{TERM–EN}$	Single–ended threshold for high–speed termination enable	–	–	450	mV
CCP	Common-point termination	–	–	60	pF

Table 65: Low–Power MIPI D–PHY Receiver (RX) DC Specifications

Parameter	Description	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	740	–	–	mV
V_{IL}	Logic 0 input voltage, not in ULP state	–	–	550	mV
$V_{IL–ULPS}$	Logic 0 input voltage, ULP state	–	–	300	mV
V_{HYST}	Input hysteresis	25	–	–	mV

Table 66: Low-Power MIPI D–PHY Receiver (RX) AC Specifications

Parameter	Description	Min	Typ	Max	Unit
T_{MIN-RX}	Minimum pulse width response	20	–	–	ns
V_{INT}	Peak interference amplitude	–	–	200	mV
f_{INT}	Interference frequency	450	–	–	MHz

MIPI Power-Up Timing

Apply power to VCC12A_MIPI*x*_TX, VCC12A_MIPI*x*_RX, , and VCC25A_MIPI*x* at least t_{MIPI_POWER} after VCC is stable. See **Power Up Sequence** on page 38 for a power-up sequence diagram.

Table 67: MIPI Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{MIPI_POWER}	Minimum time after VCC is stable before powering MIPI power supplies.	1	–	–	µs

MIPI Reset Timing

The MIPI RX and TX interfaces have two reset signals (DPHY_RSTN and RSTN) to reset the D-PHY controller logic. These signals are active low, and you should use them together to reset the MIPI interface.

The following waveform illustrates the minimum time required to reset the MIPI interface.

Figure 31: DPHY_RSTN and RSTN Timing Diagram

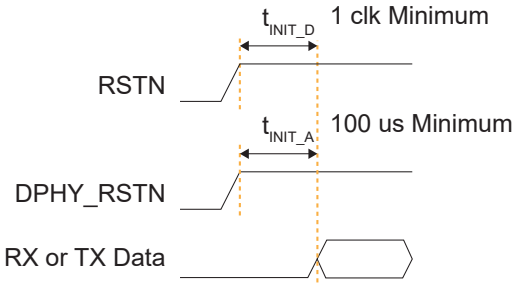


Table 68: MIPI Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{INIT_A}	Minimum time between the rising edge of DPHY_RSTN and the start of MIPI RX or TX data.	100	–	–	µs
t_{INIT_D}	Minimum time between the rising edge of RSTN and the start of MIPI RX or TX data.	1	–	–	clk

PLL Timing and AC Characteristics

The following tables describe the PLL timing and AC characteristics.

Table 69: PLL Timing (C3, C4, Q4, and I4)

Symbol	Parameter	Min	Typ	Max	Units
F_{IN} (16)	Input clock frequency from core.	10	–	330	MHz
	Input clock frequency from GPIO.	10	–	200	MHz
	Input clock frequency from LVDS.	10	–	400	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{VCO}	PLL VCO frequency for internal feedback mode.	500	–	1,600	MHz
	PLL VCO frequency for local and core feedback mode	500	–	3,600	MHz
F_{PLL}	Post-divider PLL VCO frequency if all output divider values <= 64	62.5	–	1,800	MHz
	Post-divider PLL VCO frequency if any of the output divider value > 64	62.5	–	1,400	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	100	MHz

Table 70: PLL Timing (C4L and I4L)

Symbol	Parameter	Min	Typ	Max	Units
F_{IN} (16)	Input clock frequency from core.	10	–	330	MHz
	Input clock frequency from GPIO.	10	–	200	MHz
	Input clock frequency from LVDS.	10	–	400	MHz
F_{OUT}	Output clock frequency.	0.24	–	500	MHz
F_{VCO}	PLL VCO frequency for internal feedback mode.	500	–	1,600	MHz
	PLL VCO frequency for local and core feedback mode	500	–	3,200	MHz
F_{PLL}	Post-divider PLL VCO frequency if all output divider values <= 64	62.5	–	1,600	MHz
	Post-divider PLL VCO frequency if any of the output divider value > 64	62.5	–	1,200	MHz
F_{PFD}	Phase frequency detector input frequency.	10	–	100	MHz

(16) When using the Dynamic clock source mode, the maximum input clock frequency is limited by the slowest clock frequency of the assigned clock source. For example, the maximum input clock frequency of a Dynamic clock source mode from core and GPIO is 200 MHz.

Table 71: PLL AC Characteristics[17]

Symbol	Parameter	Min	Typ	Max	Units
t_{DT}	Output clock duty cycle.	40	50	60	%
t_{OPJIT} (PK - PK) [18]	Output clock period jitter (PK-PK).	–	–	200	ps
t_{PLL_HLW}	PLL input clock from GPIO, HIGH/LOW pulse width.	2.25	–	–	ns
	PLL input clock from LVDS, HIGH/LOW pulse width.	1.13	–	–	ns
t_{ILJIT} (PK - PK)	Input clock long-term jitter (PK-PK)	–	–	800	ps
t_{LOCK}	PLL lock-in time.	–	–	0.5	ms

[17] Test conditions at 3.3 V and room temperature.
[18] The output jitter specification applies to the PLL jitter when an input jitter of 20 ps is applied.

Configuration Timing

The T13 FPGA has the following configuration timing specifications. Refer to AN 006: Configuring Trion FPGAs for detailed configuration information.

Table 72: Timing Parameters for All Modes

Symbol	Parameter	Min	Typ	Max	Units
t_{CRESET_N}	Minimum creset_n low pulse width required to trigger re-configuration.	320	–	–	ns
t_{USER}	Minimum configuration duration after CDONE goes high before entering user mode.[19][20] Test condition at 10 kΩ pull-up resistance and 10 pF output loading on CDONE pin.	12	–	[21]	µs

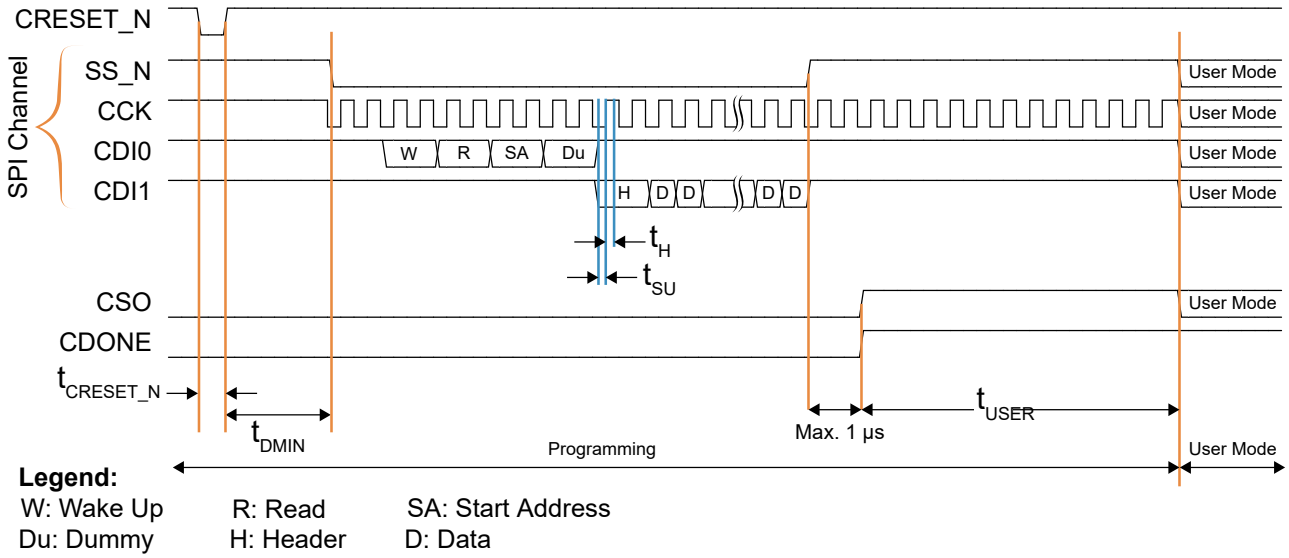
[19] The FPGA may go into user mode before t_{USER} has elapsed. However, Elitestek recommends that you keep the system interface to the FPGA in reset until t_{USER} has elapsed.

[20] For JTAG programming, the min t_{USER} configuration time is required after CDONE goes high and FPGA receives the ENTERUSER instruction from JTAG host (TAP controller in UPDATE_IR state).

[21] See **Maximum tUSER for SPI Active and Passive Modes** on page 58

SPI Active

Figure 32: SPI Active Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI active configuration.

Table 73: Active Mode Timing Parameters

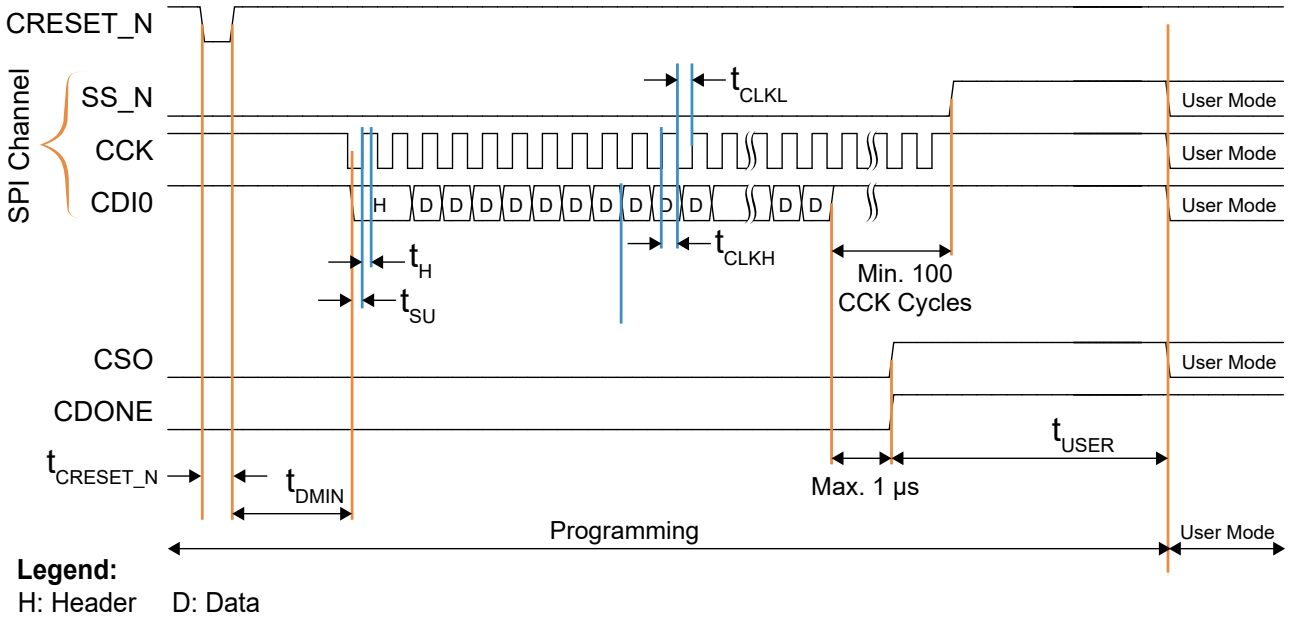
Symbol	Parameter	Frequency	Min	Typ	Max	Units
f_{MAX_M}	Active mode configuration clock frequency[22].	DIV4[23]	14	20	26	MHz
		DIV8	7	10	13	MHz
t_{SU}	Setup time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	7.5	–	–	ns
t_H	Hold time. Test condition at 3.3 V I/O standard and 0 pF output loading.	–	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	–	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 38 for details on the power-up requirements.

[22] For parallel daisy chain x2 and x4, the active configuration clock frequency, fMAX_M, must be set to DIV4.
[23] For Q100F3 packages, the total C_{LOAD} connected to each SPI pin must be less than 25 pF.

SPI Passive

Figure 33: SPI Passive Mode (x1) Timing Sequence



The JTAG pins must be inactive during SPI passive configuration.

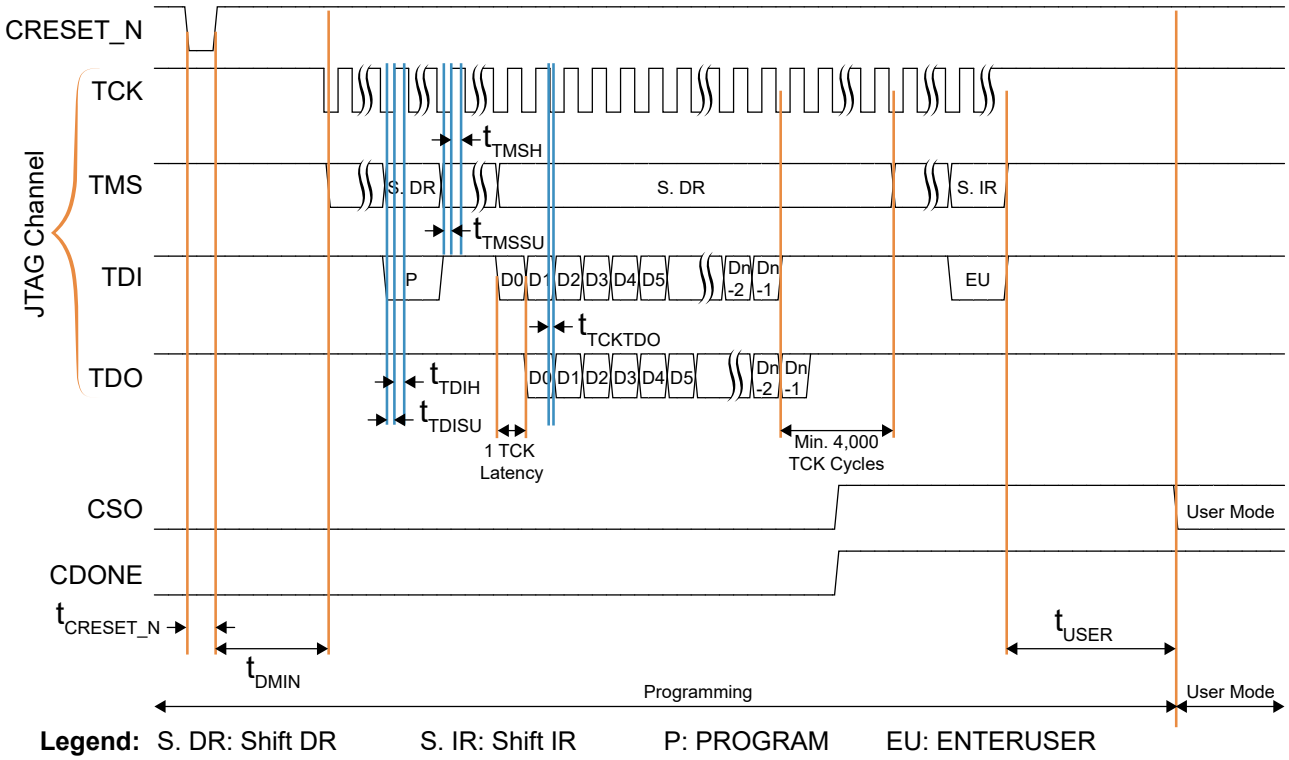
Table 74: Passive Mode Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
f_{MAX_S}	Passive mode X1 configuration clock frequency.	–	–	25	MHz
	Passive mode X2, X4 or X8 configuration clock frequency.	–	–	50	MHz
t_{CLKH}	Configuration clock pulse width high.	0.48*1/ f_{MAX_S}	–	–	ns
t_{CLKL}	Configuration clock pulse width low.	0.48*1/ f_{MAX_S}	–	–	ns
t_{SU}	Setup time.	6	–	–	ns
t_H	Hold time.	1	–	–	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 38 for details on the power-up requirements.

JTAG

Figure 34: JTAG Programming Waveform



The SPI bus must be inactive during JTAG configuration.

Important: Refer to **Power Up Sequence** on page 38 for power-up details.

Table 75: JTAG Mode Timing Parameters

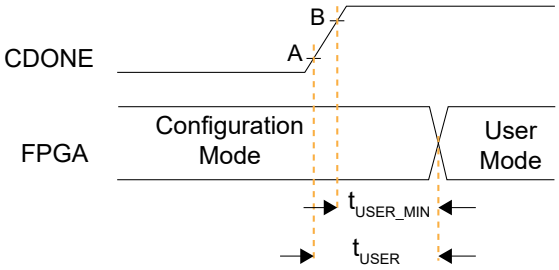
Symbol	Parameter	Min	Typ	Max	Units
f_{TCK}	TCK frequency.	–	–	25	MHz
t_{TDISU}	TDI setup time.	3.5	–	–	ns
t_{TDIH}	TDI hold time.	1	–	–	ns
t_{TMSSU}	TMS setup time.	3	–	–	ns
t_{TMSH}	TMS hold time.	1	–	–	ns
t_{TCKTDO}	TCK falling edge to TDO output.	–	–	10.5[24]	ns
t_{DMIN}	Minimum time between deassertion of CRESET_N to first valid configuration data.	1.2	–	–	µs

Note: Refer to **Power Up Sequence** on page 38 for details on the power-up requirements.

[24] 0 pf output loading.

Maximum t_{USER} for SPI Active and Passive Modes

The following waveform illustrates the minimum and maximum values for t_{USER}.



- *Point A*—User-defined trigger point to start counter on t_{USER}
- *Point B*—V_{IH} (with Schmitt Trigger) of Trion I/Os

The maximum t_{USER} value can be derived based on the following formula:

Table 76: t_{USER} Maximum

Configuration Setup	t_{USER} Maximum
Single Trion FPGA	$t_{USER} = t_{(from\ A\ to\ B)} + t_{USER_MIN}$
Slave FPGA in a dual-Trion FPGA SPI chain	
Master FPGA in a dual-Trion FPGA SPI chain	t_{USER} = (1344 / SPI_WIDTH) * CCK period + t_{USER_MIN} + $t_{(from\ A\ to\ B)}$

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 77: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates location: TL: Top left, TR: Top right, BR: bottom right
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location: 1A: Bank 1A, 3E: Bank 3E 4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)
VCCIO*xx_yy_zz*	Power	–	Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR
GND	Ground	–	Ground.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock resource. There are 5 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.
MREFCLK	Alternate	Input	MIPI TX PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single-ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.

Table 78: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

All the pins are in internal weak pull-up during configuration except for `TCK` and `TDO`.

Pins	Direction	Description	External Weak Pull- Up/ Pull Down Requirement
CDONE	I/O	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, the configuration is complete and the FPGA enters user mode. You can hold CDONE low and release it to synchronize the FPGAs entering user mode.	Pull up
CRESET_N	Input	Active-low FPGA reset and re-configuration trigger. Pulse CRESET_N low for a duration of t_{creset_N} before releasing CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	Pull up
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	Pull up
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Pull up
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Pull up
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or a test data register depending on the sequence previously applied at TMS. The shift out content is based on the issued instruction. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	Pull up

Note: All dedicated configuration pins have Schmitt Trigger buffer. See **Table 46: Single-Ended I/O and Dedicated Configuration Pins Schmitt Trigger Buffer Characteristic** on page 44 for the Schmitt Trigger buffer specifications.

Table 79: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. CBUS has an internal weak pull-up. However, Elitestek recommends that you use an external pull-up accordingly. See *Selecting the Configuration Mode* in AN 006: Configuring Trion FPGAs	Pull up or pull down[25]
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	Pull up or pull down [26]
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up. **Important:** The CCK pin in Q100F3 packages are only available in user mode when the LVDS TX resources are not in use. The CCK pin should not be toggled when any LVDS TX is used.	Optional[27]
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI (31:0) connects to the data bus in parallel.	Optional[27]
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for all configuration modes. CSI must remain high throughout all configuration modes.	Pull up
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SS_N	Input	SPI configuration mode select. The FPGA senses the value of SS_N when it comes out of reset (i.e., CRESET_N transitions from low to high). 0: SPI Passive mode; connect to external weak pull down. 1: SPI Active mode; connect to external weak pull up. In active configuration mode, SS_N is an active-low chip select to the flash device (CDI0 - CDI3).	Optional[27]
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During all configuration modes, rely on the external weak pull-up or drive this pin high.	Pull up

[25] Optional for x1 mode.
[26] Not applicable to single-image or remote update.
[27] Optional unless pull-up is required by external load.

Table 80: MIPI Pinouts (Dedicated)

n Indicates the number. *L* indicates the lane

Function	Group	Direction	Description
VCC25A_MIPI0 VCC25A_MIPI1	Power	–	MIPI 2.5 V analog power supply.
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	Power	–	MIPI 1.2 V TX analog power supply.
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	Power	–	MIPI 1.2 V RX analog power supply.
GNDA_MIPI	Ground	–	Ground for MIPI analog power supply.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	MIPI	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	MIPI	I/O	MIPI differential receive data lane.
MREFCLK	Clock	Input	MIPI PLL reference clock source.

Table 81: SPI Flash Memory Pin

Function	Direction	Description
SPI_CS_N	Input	Active-low internal SPI flash memory chip select. Available in QFP100F3 packages only.

Pin States

GPIO pins have as internal pull up/down (see **Figure 7: I/O Interface Block** on page 14), and LVDS pins used as GPIO have a weak pull up. The following table shows the pin state during reset, configuration, and when unused in user mode.

Table 82: I/O Pin States

Pin Type	During Reset (CRESET_N Low)	During Configuration (CRESET_N High, CDONE Low)	When Unused in User Mode (Default)
User Pins			
GPIO	Input tri-state with weak pull up.	Input tri-state with weak pull up.	Input tri-state with weak pull up.[28]
LVDS used as GPIO	Input tri-state with no weak pull up or pull down.	Input tri-state with no weak pull up or pull down.	Input tri-state with weak pull up.
Dual-Purpose Configuration Pins			
CSO	0	0[29]	Input tri-state with weak pull up.
NSTATUS	1	1[30]	Input tri-state with weak pull up.
CCK	Input tri-state with weak pull up.	SPI active output clock. SPI passive input with weak pull up.	Input tri-state with weak pull up.
CDI0	Input tri-state with weak pull up.	SPI active output. SPI passive input with weak pull up.	Input tri-state with weak pull up.

As shown in **Power Up Sequence** on page 38, `CRESET_N` must be kept low during power up.

Note: Refer to the following tables for details:
Table 48: Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance on page 44

Efinity Software Support

The Efinity® software provides a complete tool flow from RTL design to bitstream generation, including synthesis, place-and-route, and timing analysis. The software has a graphical user interface (GUI) that provides a visual way to set up projects, run the tool flow, and view results. The software also has a command-line flow and Tcl command console. The Efinity® software supports simulation flows using the ModelSim, NCSim, or free iVerilog simulators. An integrated hardware Debugger with Logic Analyzer and Virtual I/O debug cores helps you probe signals in your design. The software-generated bitstream file configures the T13 FPGA. The software supports the Verilog HDL, SystemVerilog, and VHDL languages.

(28) You can change it to weak pull-down in the Interface Designer.
(29) CSO is driven to 1 when the bitstream is done transmitting (CDONE = 1).
(30) NSTATUS is driven to 0 if the FPGA detects an incorrect JTAG ID or detects a CRC error.

T13 Interface Floorplan

Note: The numbers in the floorplan figures indicate the GPIO and LVDS number ranges. Some packages may not have all GPIO or LVDS pins in the range bonded out. Refer to the T13 pinout for information on which pins are available in each package.

Figure 35: Floorplan Diagram for Q100F3 Packages

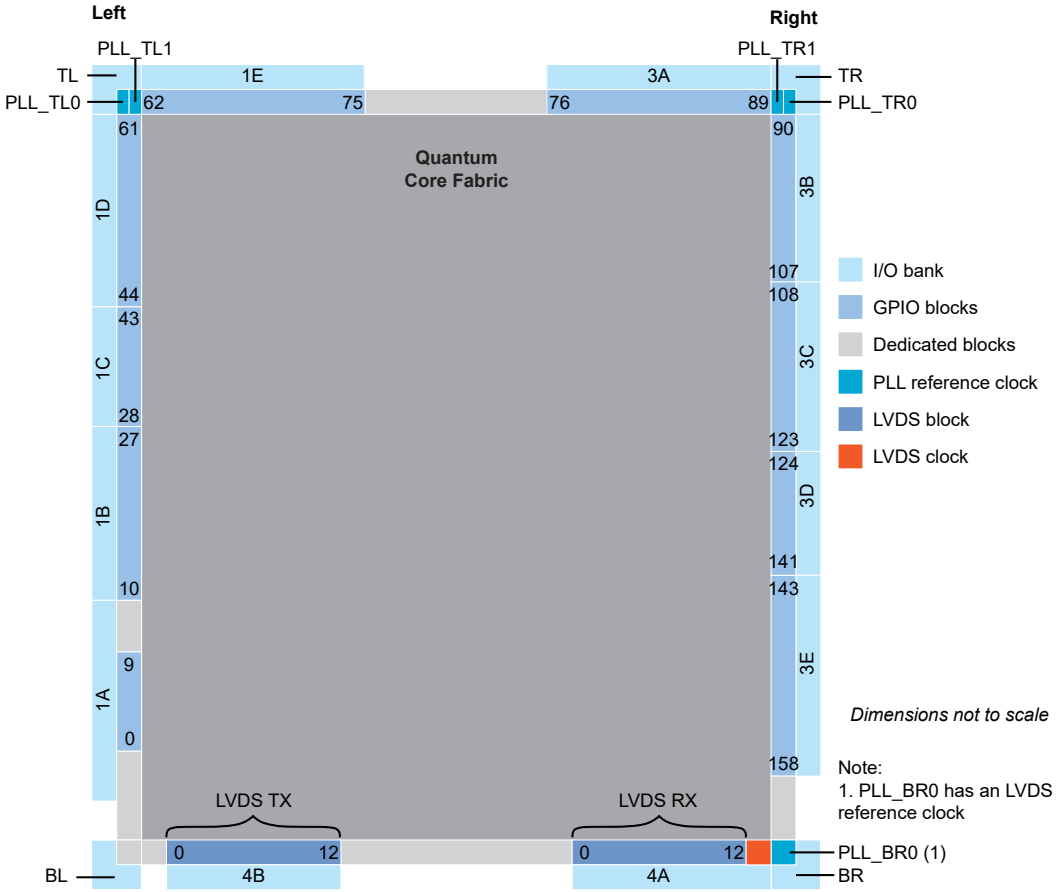


Figure 36: Floorplan Diagram for F169 Packages (with MIPI)

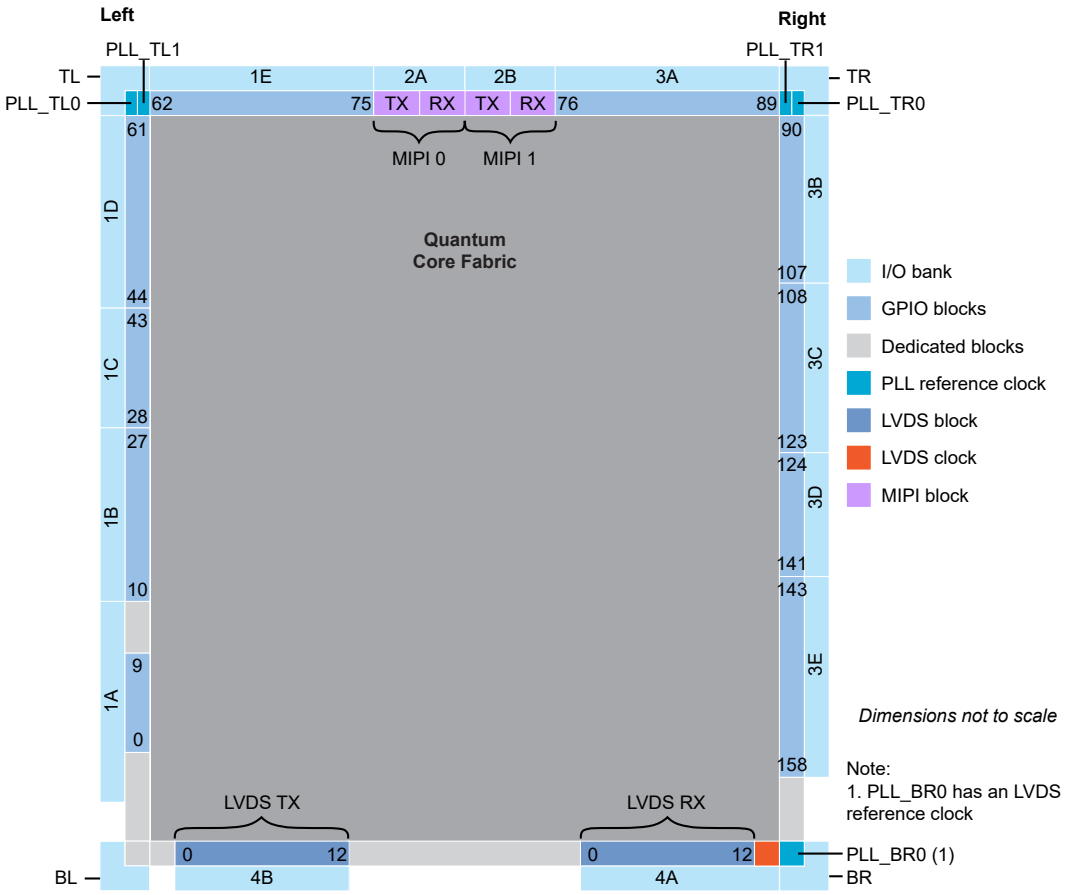
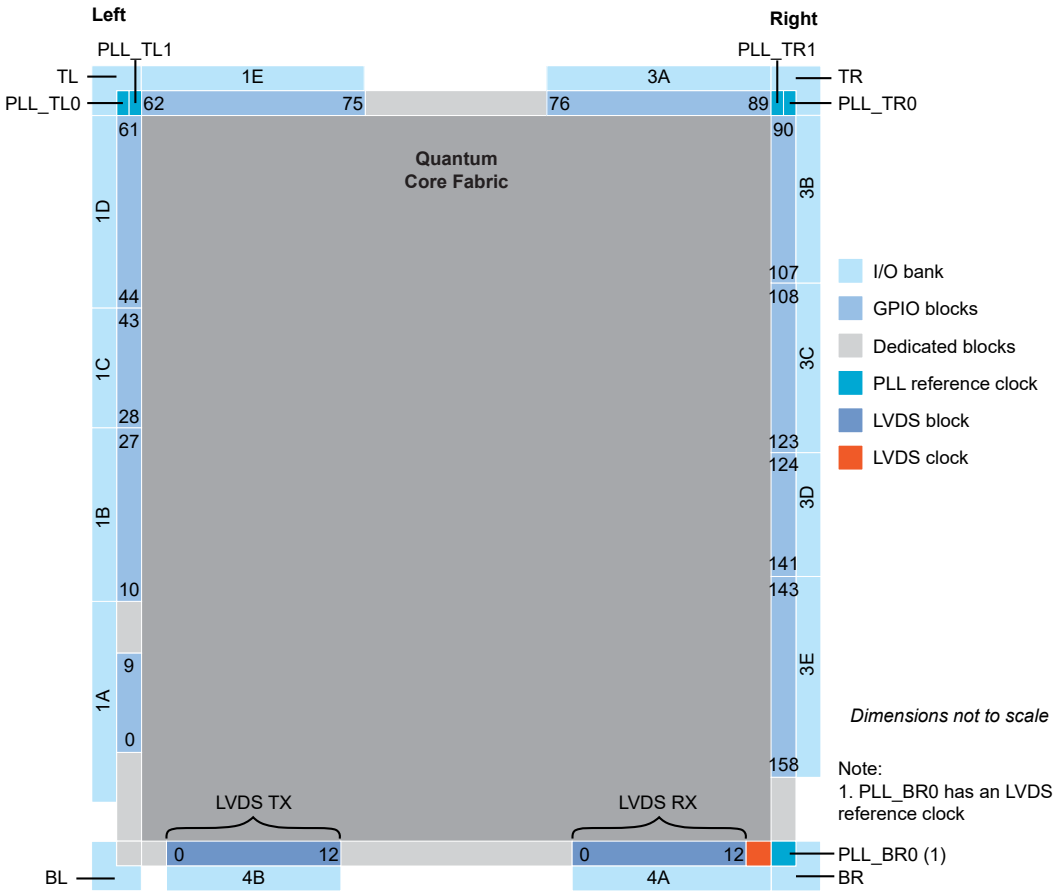


Figure 37: Floorplan Diagram for F256 Packages



Ordering Codes

Refer to the Trion Selector Guide for the full listing of T13 ordering codes.

Revision History

Table 83: Revision History

Date	Version	Description
April 2025	4.8	Fixed typo in **Table 73: Active Mode Timing Parameters** on page 55. (DOC-2500)
April 2025	4.7	Correction to **MIPI Power-Up Timing** on page 50. Updated LVDS used as GPIO state in Pin States topic. Updated configuration timing waveforms. (DOC-2325) Corrected MIPI reset timing diagram. (DOC-2323) Moved information about unused resources to **Unused Resources and Features** on page 39.
November 2024	4.6	Updated GPIO interface pin names (IN to I and OUT to O). (DOC-2086) Fixed typo in **Table 79: Dual-Purpose Configuration Pins** on page 61. (DOC-2038) Footnote added to **Table 13: PLL Signals (Interface to FPGA Fabric)** on page 18. (DOC-1939) Removed Dynamic Enable Pin Name from **Table 22: LVDS RX Settings in Efinity Interface Designer** on page 23. Pin does not exist in Trion family. (PT-2355) Added Pin States topic. (DOC-2087) SPI and JTAG pins should not be active at the same time for configuration. (DOC-2046) Renamed package prefix to match Efinity software (e.g., BGA changesd to F).
February 2024	4.5	Updated SPI passive timing waveform. Added note about external DC-biased circuit is required if the incoming LVDS signals are AC-coupled and link to Trion Hardware Design Checklist and Guidelines. (DOC-1532)
October 2023	4.4	Added note about maximum C_{LOAD} for SPI pins for DIV4 SPI active mode in QFP100F3 packages. (DOC-1423)
October 2023	4.3	Added LVDS RX Static Mode Delay Setting. (DOC-1473) Updated Maximum Toggle Rate table by adding recommendation to run simulation for actual taggle rate. (DOC-1468) Updated 2.5 V and 1.8 LVCMOS Single-Ended I/O Internal Weak Pull-Up and Pull-Down Resistance. (DOC-1476) Updated absolute maximum ratings for VCCIO1A_1B_1C and T_J, removed preliminary notes, and updated SPI flash block topic for in QFP100F3 packages. (DOC-1503)
September 2023	4.2	Updated maximum LVDS toggle rate for QFP100F3 packages. (DOC-1447) Updated CCK pin description. (DOC-1447)
June 2023	4.1	Updated SPI Flash Memory Signals table.
June 2023	4.0	Removed t_{LVDS_DT} and t_{INDT} specs, and replaced with t_{PLL_HLW} and t_{LVDS_CPA}. (DOC-1189) Updated PLL LOCKED signal description. (DOC-1208)
April 2023	3.9	Added support for Q100F3 packages. Corrected t_{LVDS_SU} and t_{LVDS_HD} specs (DOC-1070) Updated PLL RSTN signal description about de-asserting only when CLKIN is stable. (DOC-1226)
February 2023	3.8	Updated t_{LVDS_skew} specs. (DOC-1111) Updated t_{LVDS_SU} specs (DOC-1070) Updated power up sequence diagram. (DOC-954) Added note to use LVDS blocks from the same side to minimize skew. (DOC-1150) Updated Advanced PLL Settings table descriptions. (DOC-945)
November 2022	3.7	Added note recommending up to only 2 cascading PLLs. (DOC-931) Corrected I_{OH} and I_{OL} in buffer drive strength characteristic specifications. (DOC-933) Updated F_{VCO}, F_{PLL}, and F_{PFD} PLL Timing parameter specifications and PLL Interface Designer Settings - Manual Configuration Tab notes. (DOC-1019) Added tLVDS_SU, tLVDS_HD specs and LVDS RX timing waveforms.

Date	Version	Description
September 2022	3.6	Removed PLL_EXTFB from alternative input. (DOC-849) Updated Advanced PLL LOCKED signal description. (DOC-763)
April 2022	3.5	Updated test condition load to maximum load in Maximum Toggle Rate Table. (DOC-781) Updated Connection Requirements for Unused Resources table by specifying VCC value. (DOC-770) Updated note about leaving at least 2 pairs of unassigned LVDS pins between any GPIO and LVDS in the same device side. (DOC-769)
March 2022	3.4	Updated behaviour description for GPIO and LVDS as GPIO pins during configuration, and unused GPIO pins during user mode. (DOC-720) Added note about the block RAM content is random and undefined if it is not initialized. (DOC-729) Updated power supply ramp rate and power up sequence diagram. (DOC-631)
January 2022	3.3	Added LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics.
January 2022	3.2	Corrected power supply ramp rate. (DOC-699)
January 2022	3.1	Removed LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength Characteristics. (DOC-679) Added Output Differential Voltage with Reduce VOD Swing option enabled specs. (DOC-648) Added maximum I/O pin input current, I_{IN}, and maximum per bank specs. (DOC-652) Added PLL input clock duty cycle, t_{INDT}, specs. (DOC-661) Updated CDONE pin direction as bidirectional. (DOC-672)
November 2021	3.0	Added storage temperature, T_{STG} spec. (DOC-560) Updated maximum JTAG mode TCK frequency, f_{TCK}. (DOC-574) Updated CSI pin description. (DOC-546) Updated LVDS Pins Configured as Single-Ended I/O Buffer Drive Strength specifications. (DOC-578) Update LVDS standard compliance which is TIA/EIA-644. (DOC-592) Updated t_{CLKH} and t_{CLKL}, and corrected SPI Passive Mode (x1) Timing Sequence waveform. (DOC-590) Updated REF_RES_*xx* description. (DOC-602, DOC-605) Updated Maximum Toggle Rate table. (DOC-630) Updated minimum Power Supply Ramp Rates and Power Up Sequence figure. (DOC-631)
September 2021	2.14	Added Single-Ended I/O and LVDS Pins Configured as Single-Ended I/O Rise and Fall Time specs. (DOC-522) Added note to Active mode configuration clock frequency stating that for parallel daisy chain x2 and x4 configuration, f_{MAX_M}, must be set to DIV4. (DOC-528) Added Global Clock Location topic. (DOC-532) Added Maximum t_{USER} for SPI Active and Passive Modes topic. (DOC-535)
August 2021	2.13	Added internal weak pull-up and pull-down resistor specs. (DOC-485) Updated table title for Single-Ended I/O Schmitt Trigger Buffer Characteristic. (DOC-507) Added note in Pinout Description stating all dedicated configuration pins have Schmitt Trigger buffer. (DOC-507)
June 2021	2.12	Updated CRESET_N pin description. (DOC-450)
April 2021	2.11	Updated PLL specs; t_{ILJIT} (PK - PK) and t_{DT}. (DOC-403) Added note about limiting number of LVDS as GPIO output and bidirectional per I/O bank to avoid switching noise. (DOC-411)
March 2021	2.10	Added LVDS TX reference clock output duty cycle and lane-to-lane skew specs. (DOC-416)
March 2021	2.9	Added automotive speed grade (Q4) specs for F169 package. (DOC-399)
February 2021	2.8	Added I/O input voltage, V_{IN} specification. (DOC-389) Added LVDS TX data and timing relationship waveform. (DOC-359) Added LVDS RX I/O electrical specification waveform. (DOC-346)

Date	Version	Description
December 2020	2.7	Updated NSTATUS pin description. (DOC-335) Added data for C4L and I4L DC speed grades. (DOC-268) Updated PLL reference clock input note by asking reader to refer to PLL Timing and AC Characteristics. (DOC-336) Added other PLL input clock frequency sources in PLL Timing and AC Characteristics. (DOC-336) Removed OE and RST from LVDS block as they are not supported in software. (DOC-328) Added a table to Power Up Sequence topic describing pin connection when PLL, GPIO, or MIPI is not used. (DOC-325) Updated f_{MAX_S} for passive configuration modes. (DOC-350) Updated f_{MAX_S} for passive configuration modes. (DOC-350)
September 2020	2.6	Updated pinout links. Corrected speed grades for single-ended I/O and LVDS configured as single-ended I/O f_{MAX}.
August 2020	2.5	Update MIPI TX and RX Interface Block Diagram to include signal names. Updated REF_CLK description for clarity. Added recommended operating conditions and f_{MAX} for C4L and I4L speed grades. Updated t_{USER} timing parameter values and added a note about the conditions for the values. Updated description for GPIO pins state during configuration to exclude LVDS as GPIO. Added f_{MAX} for single-ended I/O and LVDS configured as single-ended I/O. Added maximum power supply current transient during power-up.
July 2020	2.4	Removed preliminary note from MIPI electrical specifications and timing. These specifications are final. Updated timing parameter symbols in boundary scan timing waveform to reflect JTAG mode parameter symbols. Added supported GPIO features. Updated the maximum F_{VCO} for PLL to 1,600 MHz. Updated the C divider requirement for the 90 degrees phase shift in the PLL Interface Designer Settings - Manual Configuration Tab. Updated LVDS electrical specifications note about RX differential I/O standard support, and duplicated the note in LVDS functional description topic. Added note to LVDS RX interface block diagram. Added note to recommended power-up sequence about MIPI power guideline. Updated I/O bank names from TL_CORNER, BL_CORNER, TR_CORNER, and BR_CORNER to TL, BL, TR, and BR respectively. Updated the term DSP to multiplier. Updated power up sequence description about holding CRESET_N low. Updated PLLCLK pin name to PLL_CLKIN. Added PLL_EXTFB and MIPI_CLKIN as an alternative input in GPIO signals table for complex I/O buffer. Updated PLL names in PLL reference clock resource assignments. Updated supported configuration modes. Updated typical leakage current to 6.8 mA and add a note stating it is applicable to F256 package.
February 2020	2.3	Added f_{MAX} for DSP blocks and RAM blocks. In MIPI RX and TX interface description, updated maximum data pixels for RAW10 data type. Added MIPI reset timing information. Added Trion power-up sequence. MIPI power-up moved to this topic. VCC12A_MIPI_TX, VCC12A_MIPI_RX maximum recommended operating condition changed to 1.25 V. Added number of global clocks and controls that can come from GPIO pins to package resources table.

Date	Version	Description
December 2019	2.2	Updated PLL Interface Designer settings. Removed MIPI data type bit settings. Refer to AN 015: Designing with the Trion MIPI Interface for the bit settings. Removed DIV1 and DIV2 active mode configuration frequencies; they are not supported. Added note to LVDS electrical specifications about RX differential I/O standard support.
October 2019	2.1	Added explanation that 2 unassigned pairs of LVDS pins should be located between and GPIO and LVDS pins in the same bank. Updated the reference clock pin assignments for TL_PLL0 and TL_PLL1. Added waveforms for configuration timing.
August 2019	2.0	Updated MIPI interface description. Under Ordering Codes, linked to Trion FPGA Selector Guide.
May 2019	1.0	Updated MIPI description, DC characteristics, and pin information. Updated timing specifications. Added information on the signal interface.
January 2019	0.5	Added information on DDIO support.
December 2018	0.4	Updated the package options.
November 2018	0.3	Added GNDA_*xx* (PLL analog ground) to pinout. Change VSS*xx*A_MIPI pinout to GND*xx*A_MIPI. Updated PLL block diagram and clarified feedback paths. Added floorplan information. Updated pinout table. Updated packaging options.
October 2018	0.2	Updated LVDS serialization factors.
October 2018	0.1	Initial release.